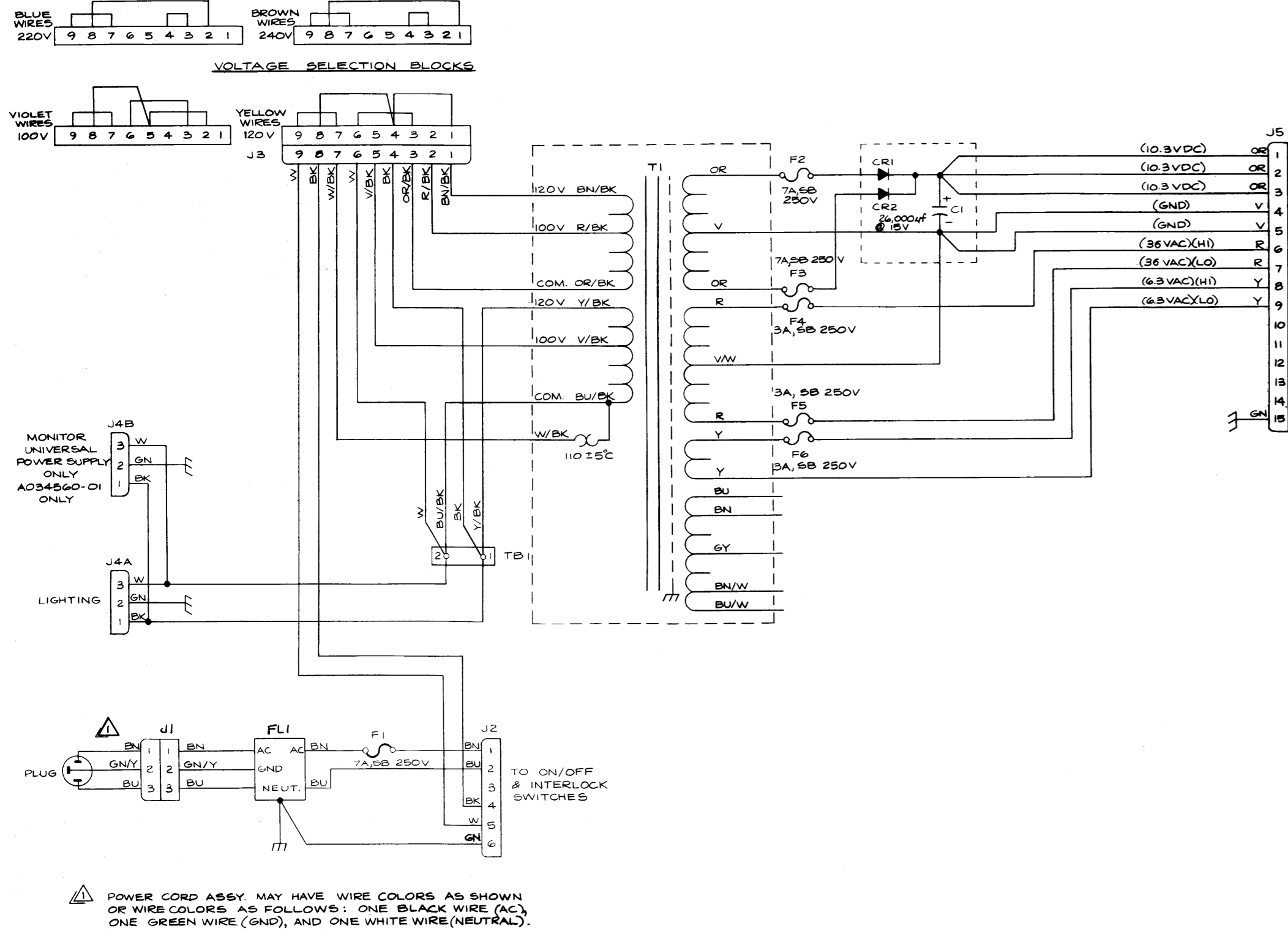


POWER SUPPLY WIRING DIAGRAM (034633-01 A)



REGULATOR/AUDIO PCB SCHEMATIC (034485-01 C)

Regulator/Audio PCB 034485-01 A

The Regulator/Audio PCB has the dual functions of regulating the +5 VDC logic power to the game PCB and amplifying the audio from the game PCB.

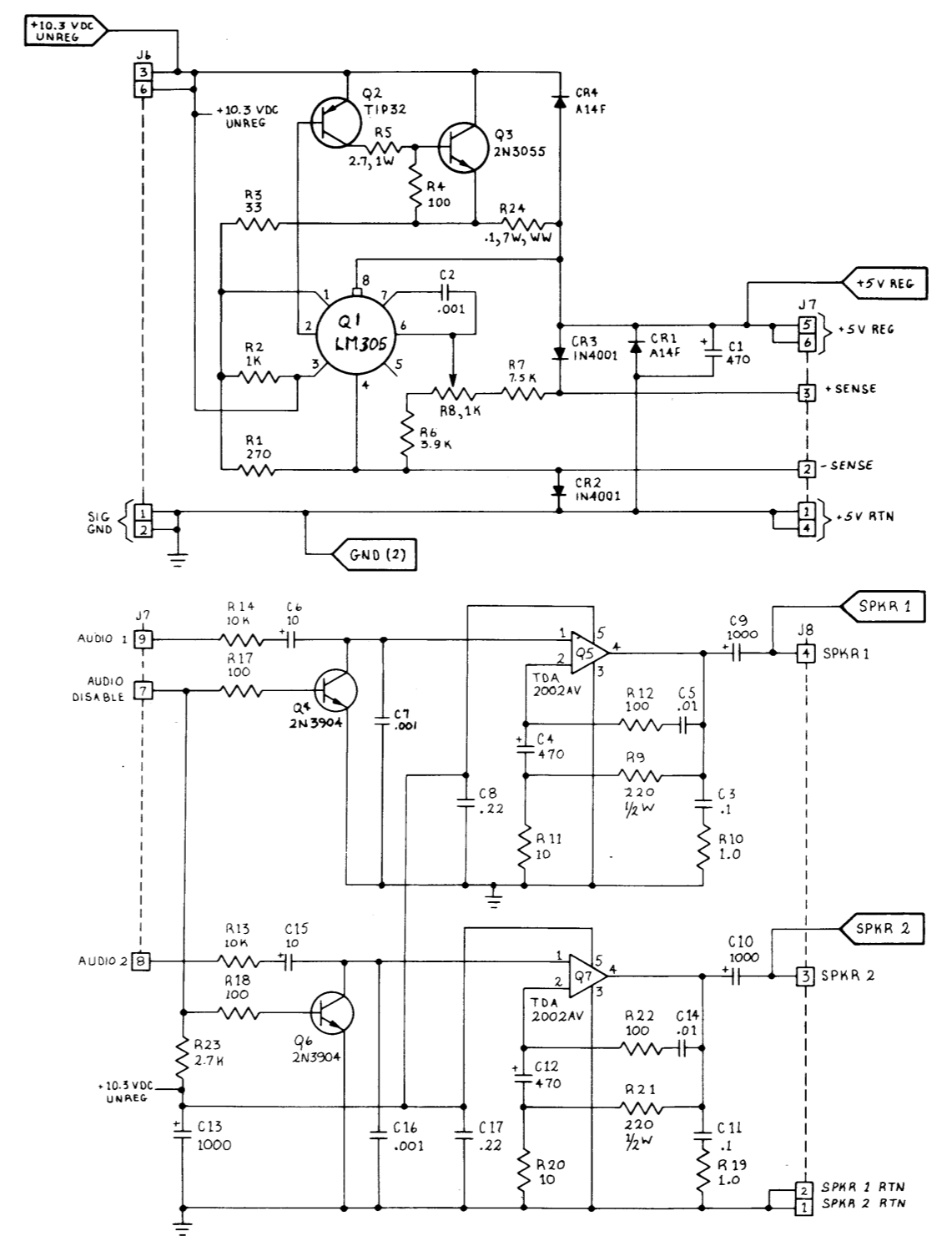
Regulator Circuit

The regulator consists of voltage regulator Q1, current source power transistor Q3 and Q3's bias transistor Q2. The regulator accurately regulates the logic power input to the game PCB by monitoring the voltage through high impedance inputs +SENSE and -SENSE. The inputs are directly from the +5 VDC and ground inputs to the game PCB. Therefore, the regulator regulates the voltage on the game PCB. This eliminates a reduced voltage due to IR buildup on the wire harness between the regulator and the game PCB. Variable resistor R8 is adjusted for the +5 VDC on the game PCB. Once adjusted, the voltage at the input of the game PCB will remain constant at this voltage.

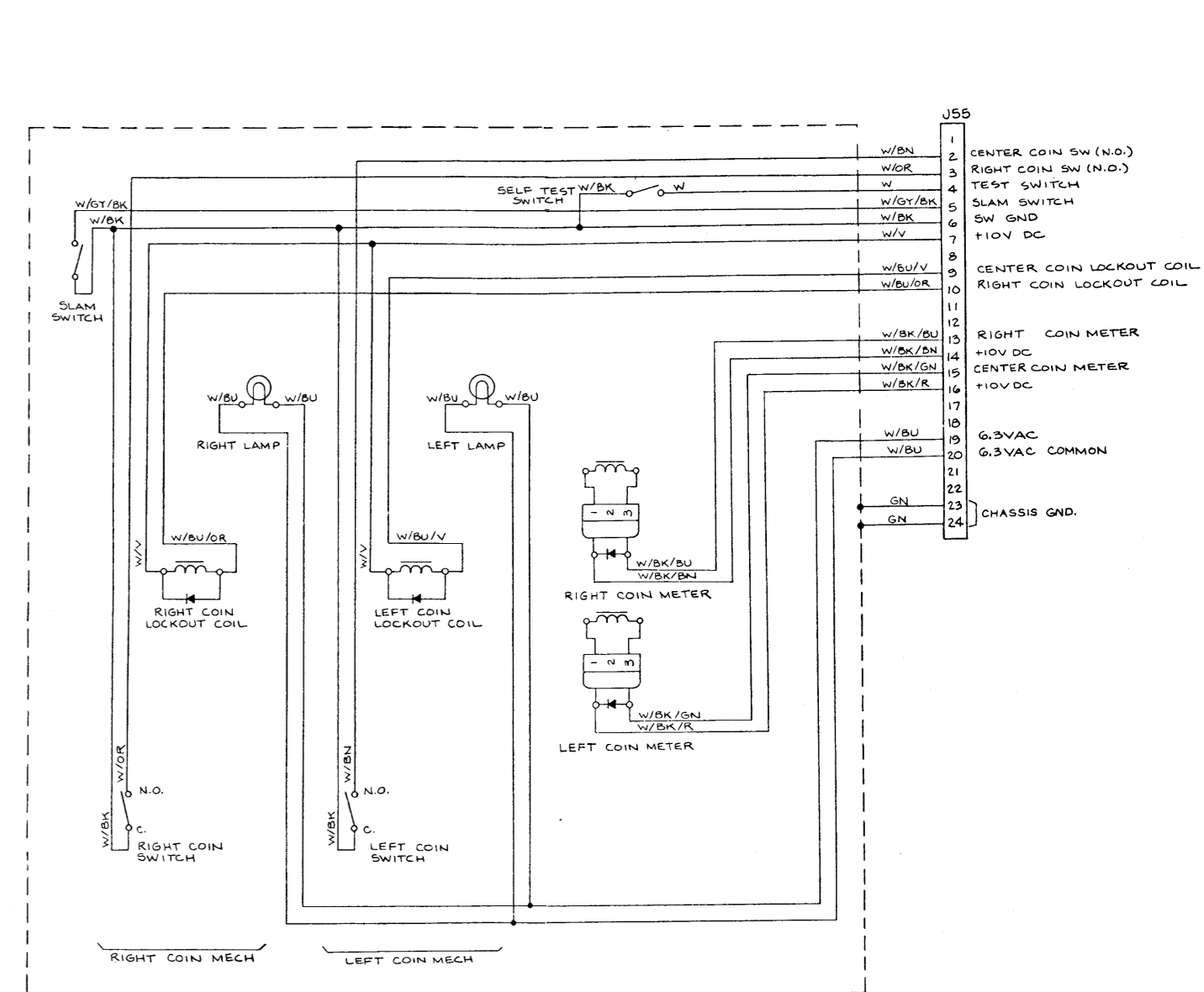
- Regulator Adjustment**
1. Connect a voltmeter between +5 V and GND test points of the game PCB.
 2. Adjust variable resistor R8 on the Regulator/Audio PCB for +5 VDC reading on the voltmeter.
 3. Connect a voltmeter between +5 V REG and GND on the Regulator/Audio PCB. Voltage reading shall not be greater than +5.5 VDC. If greater, try cleaning edge connectors on both the game PCB and the Regulator/Audio PCB.
 4. If cleaning PCB edge connectors doesn't decrease voltage difference, connect minus lead of voltmeter to GND test point of Regulator/Audio PCB and plus lead to GND test point of game PCB. Note the voltage. Now connect minus lead of voltmeter to +5 REG test point on Regulator/Audio PCB and plus lead to +5 V test point on game PCB. From this you can see which harness circuit is dropping the voltage. Troubleshoot the appropriate harness wire or harness connector.

Audio Circuit

The audio circuit contains two independent audio amplifiers. Each amplifier consists of a TDA2002AV amplifier with a gain of ten. The AUDIO DISABLE input from the game PCB inhibits both amplifiers from generating any audio during the attract mode.

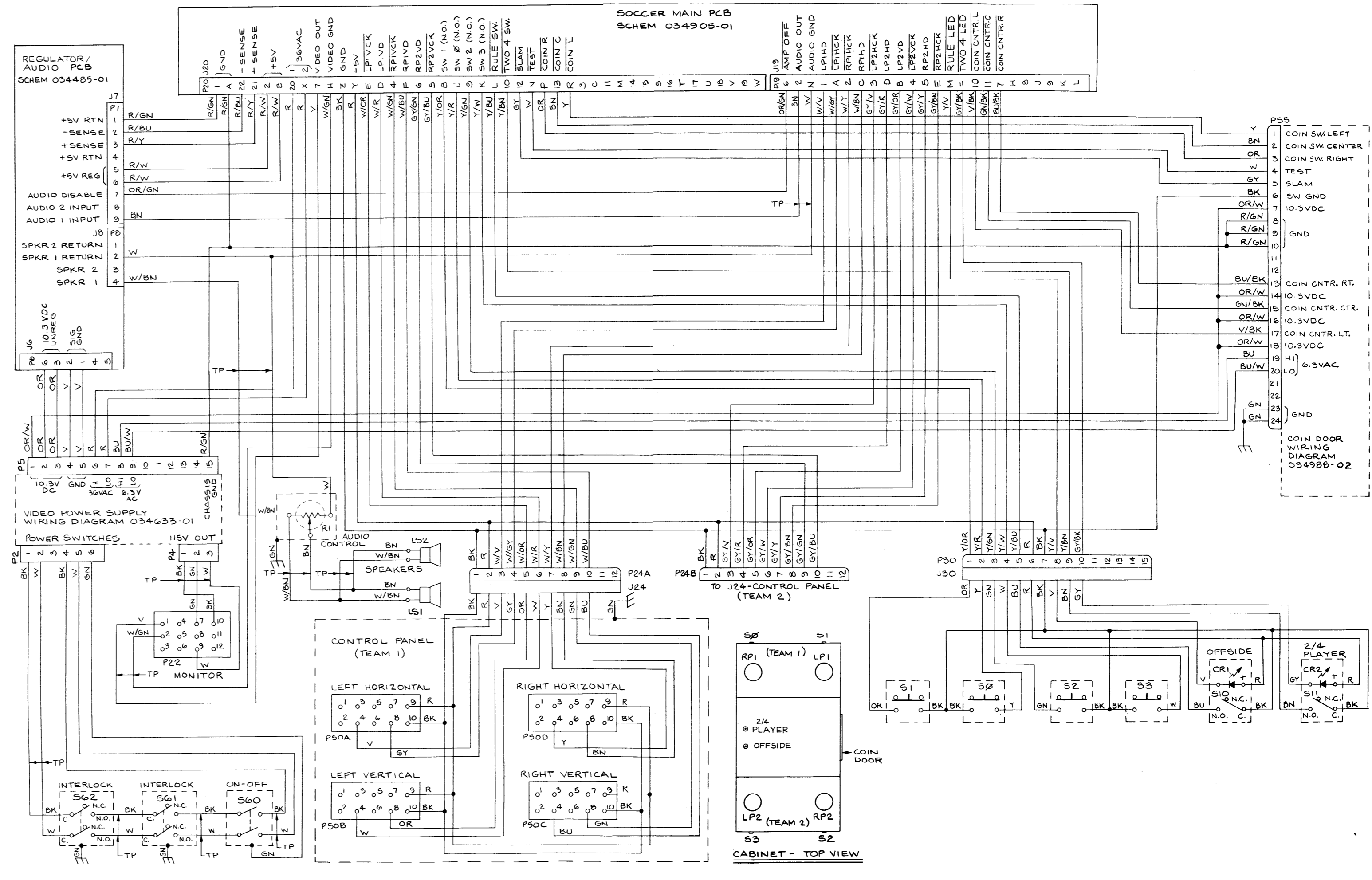


COIN DOOR SCHEMATIC (034988-02 A)



▢ denotes a test point

GAME WIRING DIAGRAM (035197-01 A)

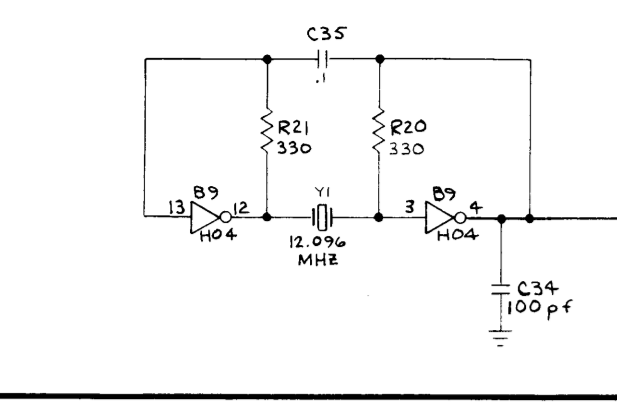


Drawing Package Supplement
to
ATARI SOCCER™
Operation, Maintenance, and Service Manual

- Contents of this Drawing Package**
- Game Wiring Diagram Sheet 1, Side A
 - Microcomputer, Clock, and Sync Sheet 1, Side B
 - Video Generator and Alphanumerics Generator Sheet 2, Side A
 - Switch Inputs, Coin Counter, and LED Outputs Sheet 2, Side B



CLOCK



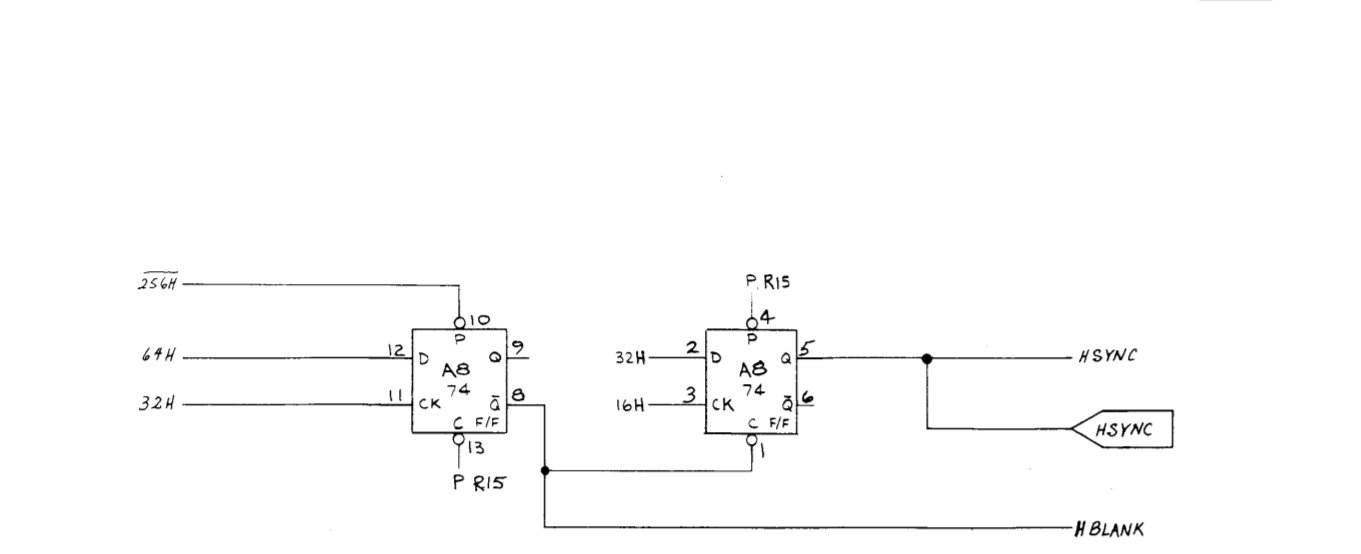
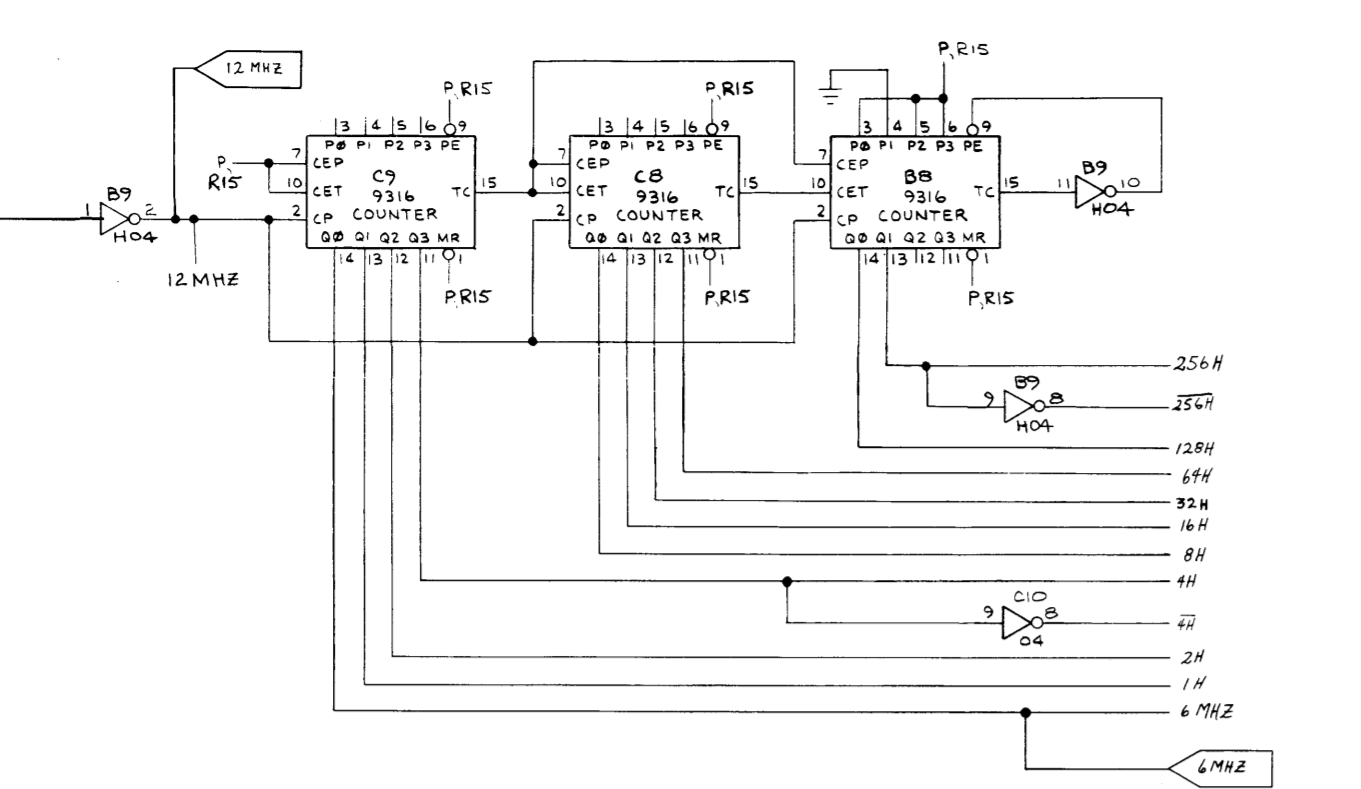
The basic frequency of the sync generator is a 12.096 MHz clock, generated by crystal Y1. The output of the oscillator, viewed with an oscilloscope, is a signal with a period of 83 nanoseconds.

The oscillator frequency is divided down by binary counters C9, C3, and B8. These provide various horizontal synchronization frequencies (1H thru 256H). The final output of the horizontal counting chain is 256H. This signal is, in effect, a division of the oscillator frequency by 768, or 15,750 Hz. The period of 256H is about 63.5 microseconds. The 256H signal, as well as other horizontal signals, are used to generate H BLANK and H SYNC timing pulses.

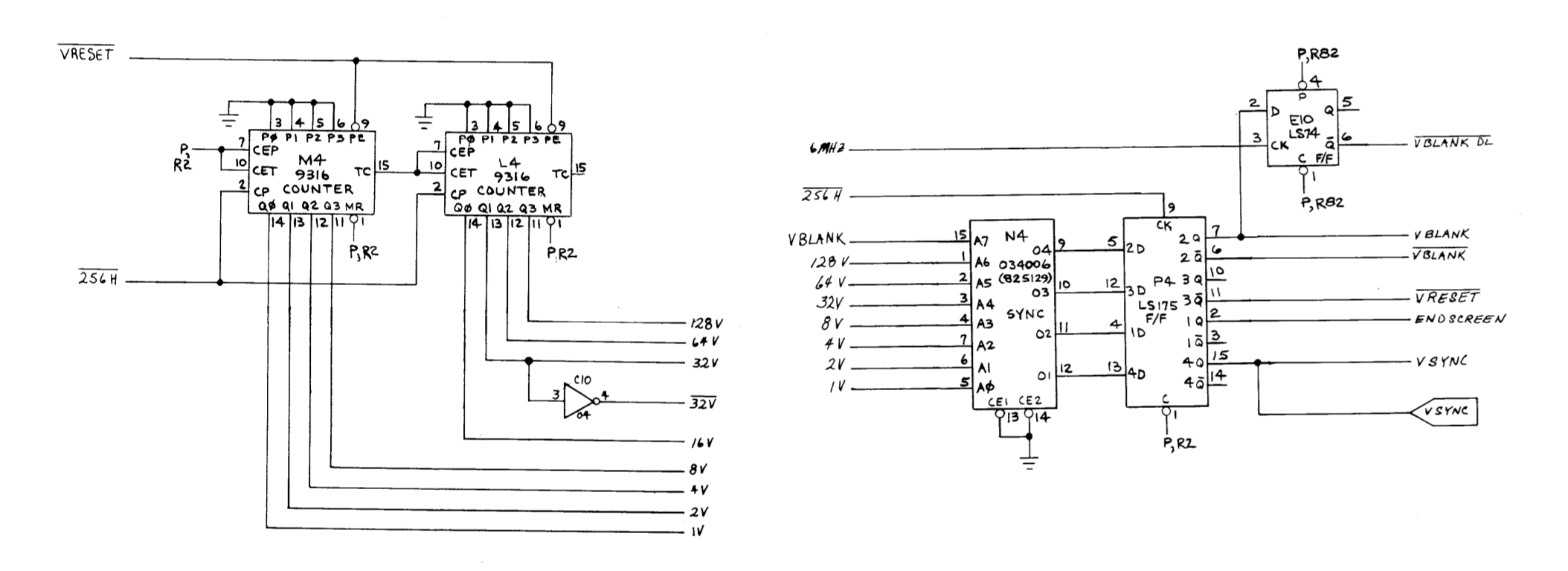
The 256H signal is used to generate vertical sync signals 1V thru 128V. The 128V signal is, in effect, a division of the 256H frequency by 262. This results in the final output of the counters of 60 Hz (16.6 milliseconds). The various vertical sync signals address sync PROM N4 whose data is latched at the output of P4.

The end result of the horizontal and vertical timing waveform is to synchronize the TV monitor display. This display consists of 262 horizontal lines per frame, only 240 lines are visible, since the last 22 lines occur during vertical blanking. Each line is equivalent to 768 clock pulses. Each frame is repeated 60 times per second, providing the necessary frequency of display refresh for a stable, non-flickering display.

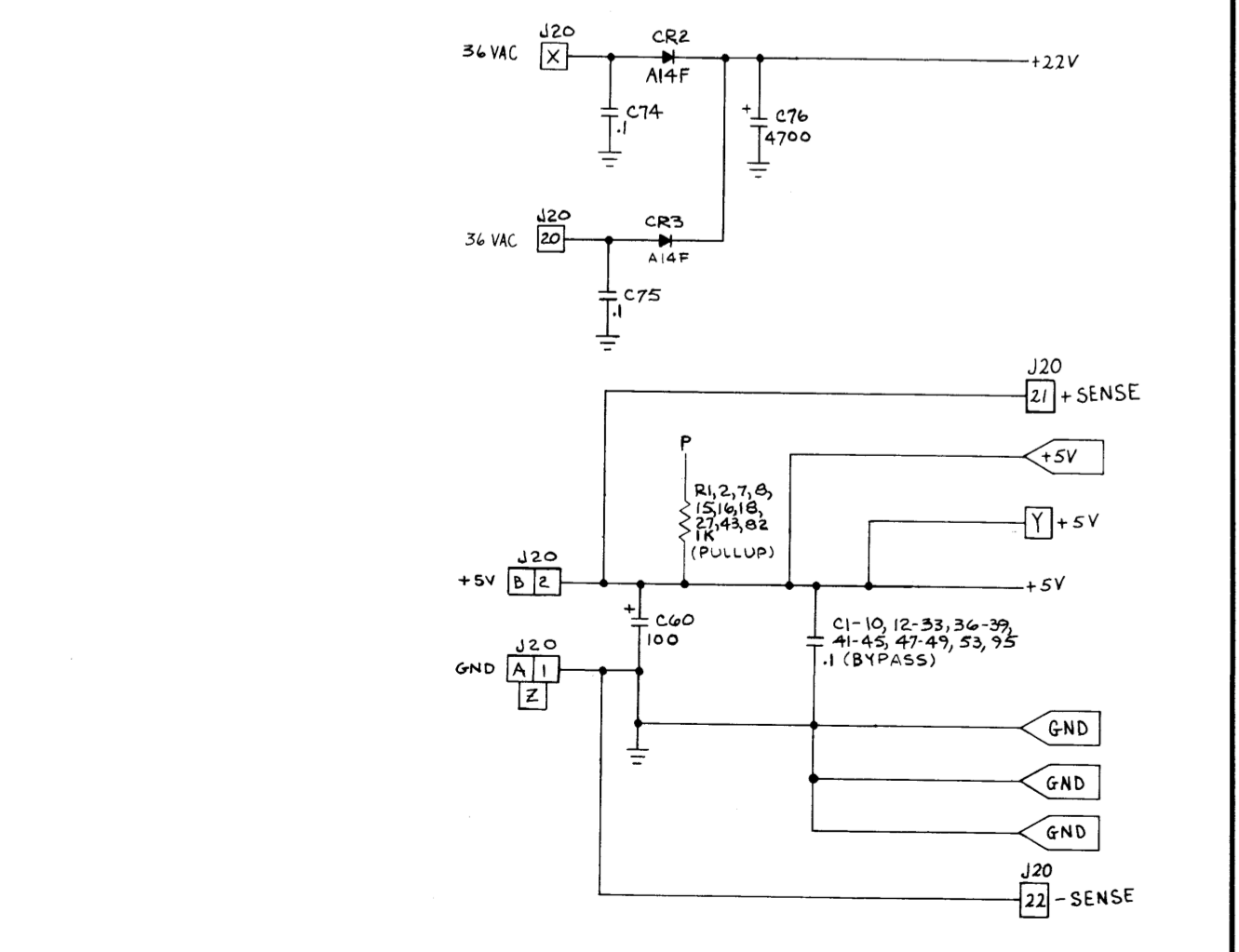
HORIZONTAL SYNC



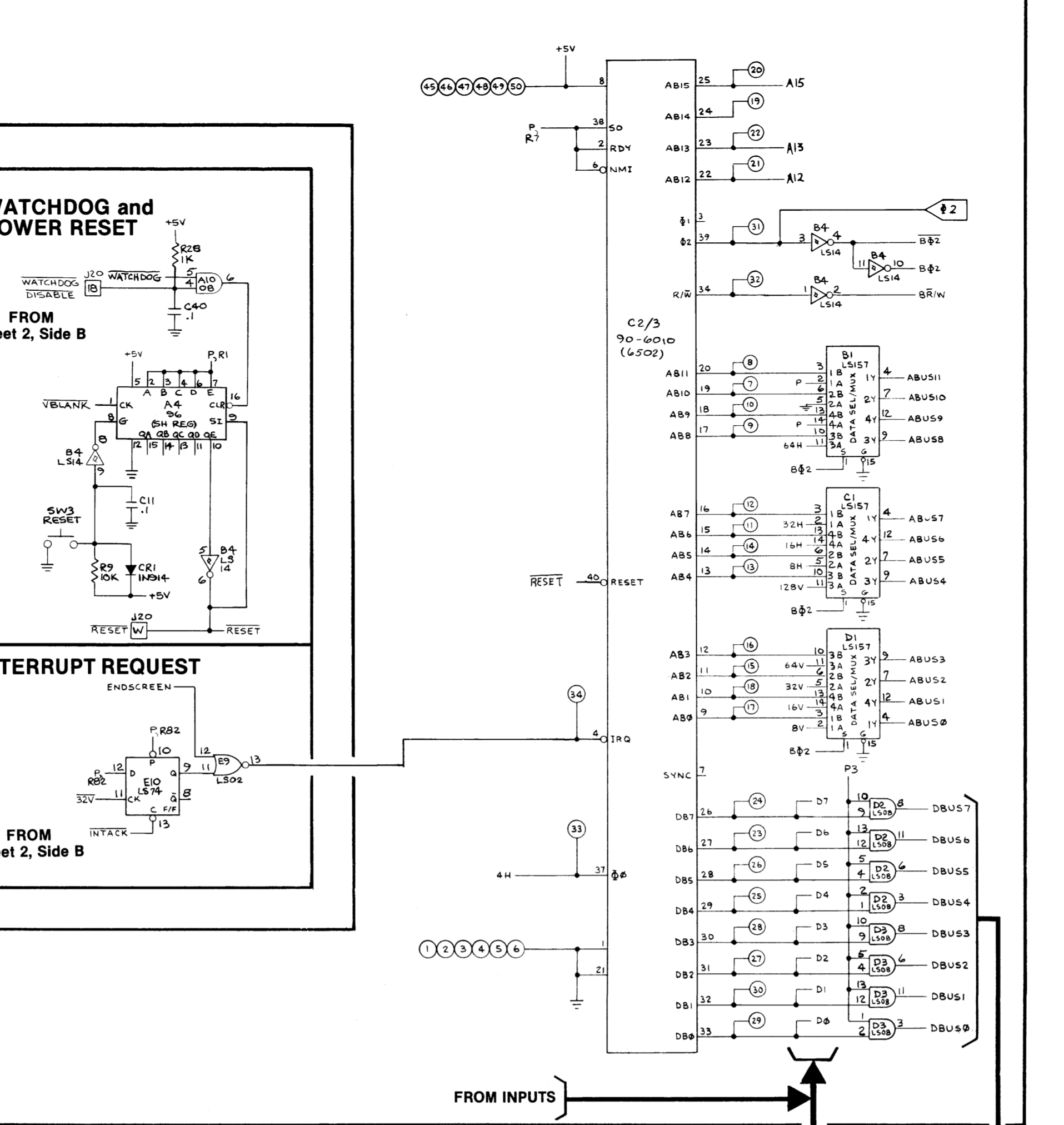
VERTICAL SYNC



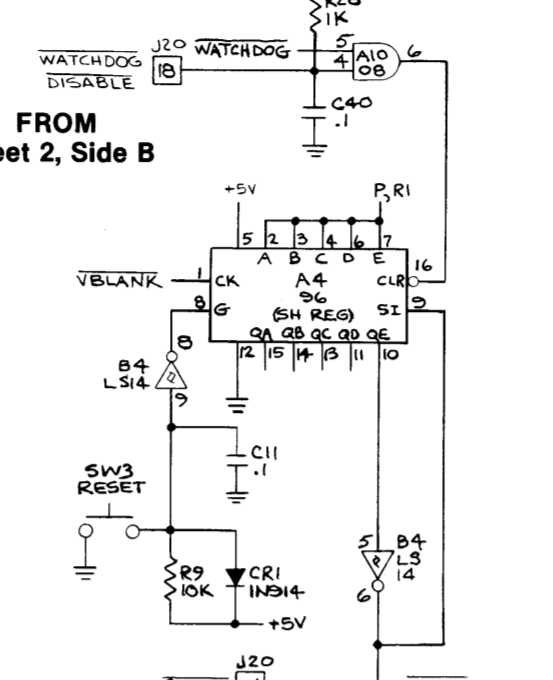
POWER INPUT



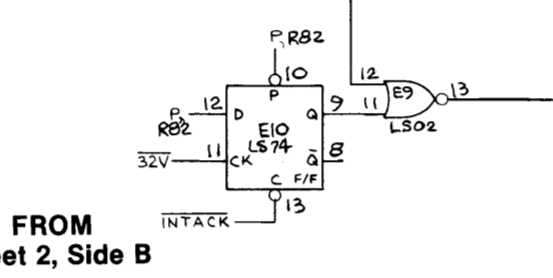
MICROPROCESSOR



WATCHDOG and POWER RESET



INTERRUPT REQUEST



The microprocessor controls all circuits on the game PCB, excluding the Sync Circuit and Watchdog and Power Reset Circuit. The Sync Circuit provides 4H (750 KHz) for the 40 clock input to the microprocessor.

WATCHDOG pulse is not received before the shift register shifts a high to QE, RESET goes low, causing the microprocessor to jump to its initialization sequence.

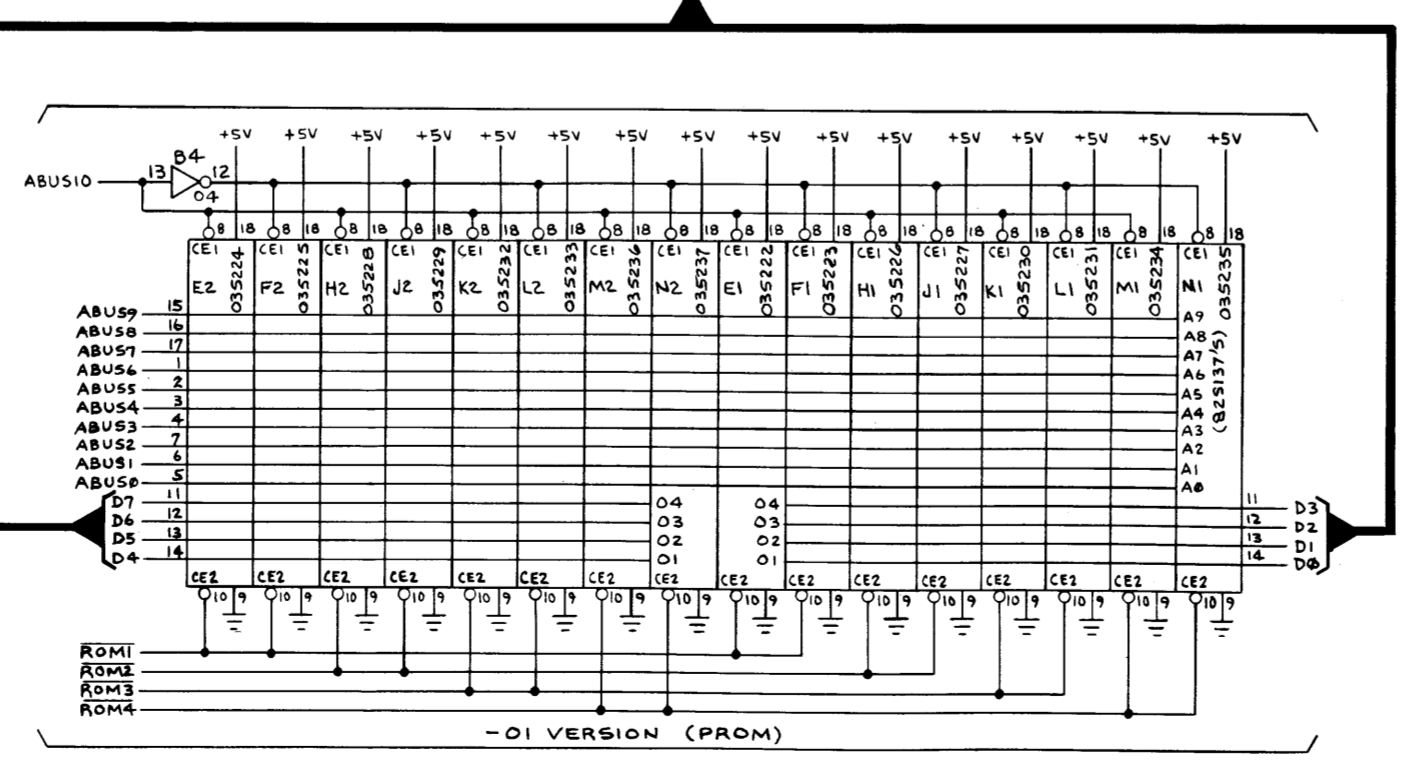
Flip-flop E10 provides an interrupt request (IRQ) input to the microprocessor. The IRQ is a timing signal used by the microprocessor.

Address bus ABUS0 thru ABUS11 is selected from either address lines AB0 thru AB11 from the microprocessor, or from various horizontal and vertical sync signals. This arrangement makes it possible for the microprocessor to write data into or read data out of the RAM when Bø2 is high. When Bø2 is low, data is read out of the RAM by the alphanumeric generator.

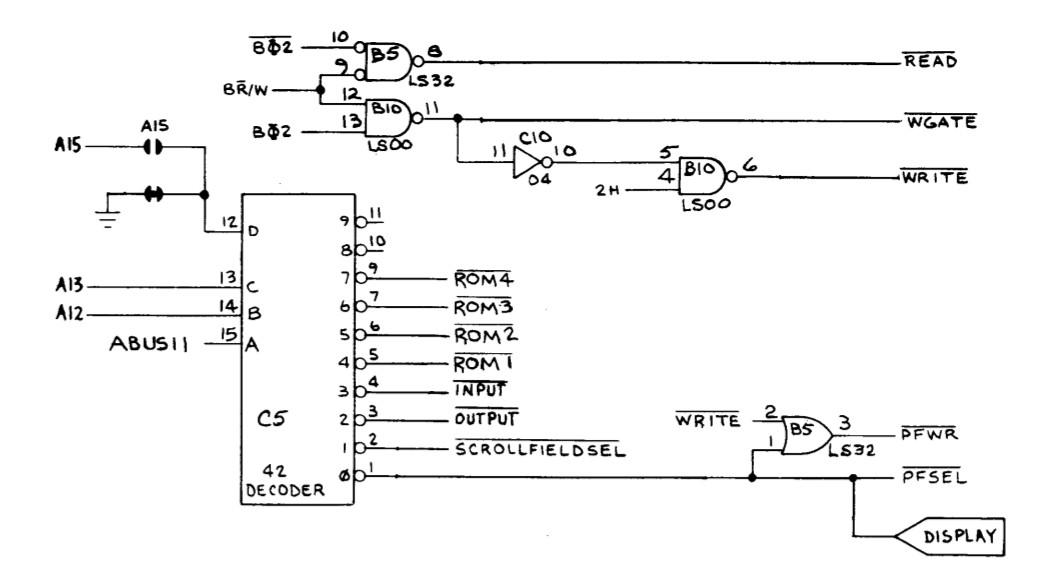
ROM/PROM MEMORY

Your Atari Soccer game PCB may contain one of several possible program memory chips sets. The -01 version of the PCB contains 16 PROMs for the memory.

The -02 version contains 4 ROM chips for the memory. A third possibility would be a mixture of ROMs and PROMs. For information regarding which ROMs are equivalent to which PROMs, see the illustrated Parts Catalog chapter of the game manual.



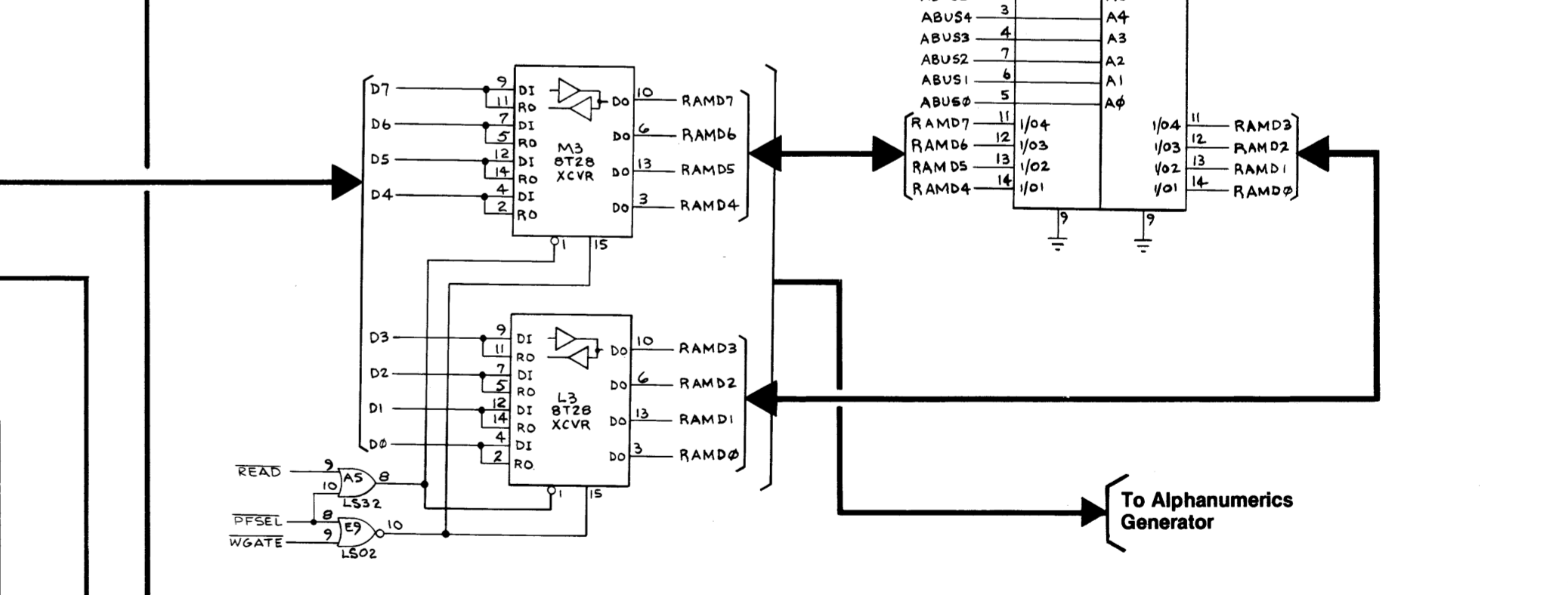
ADDRESS DECODER

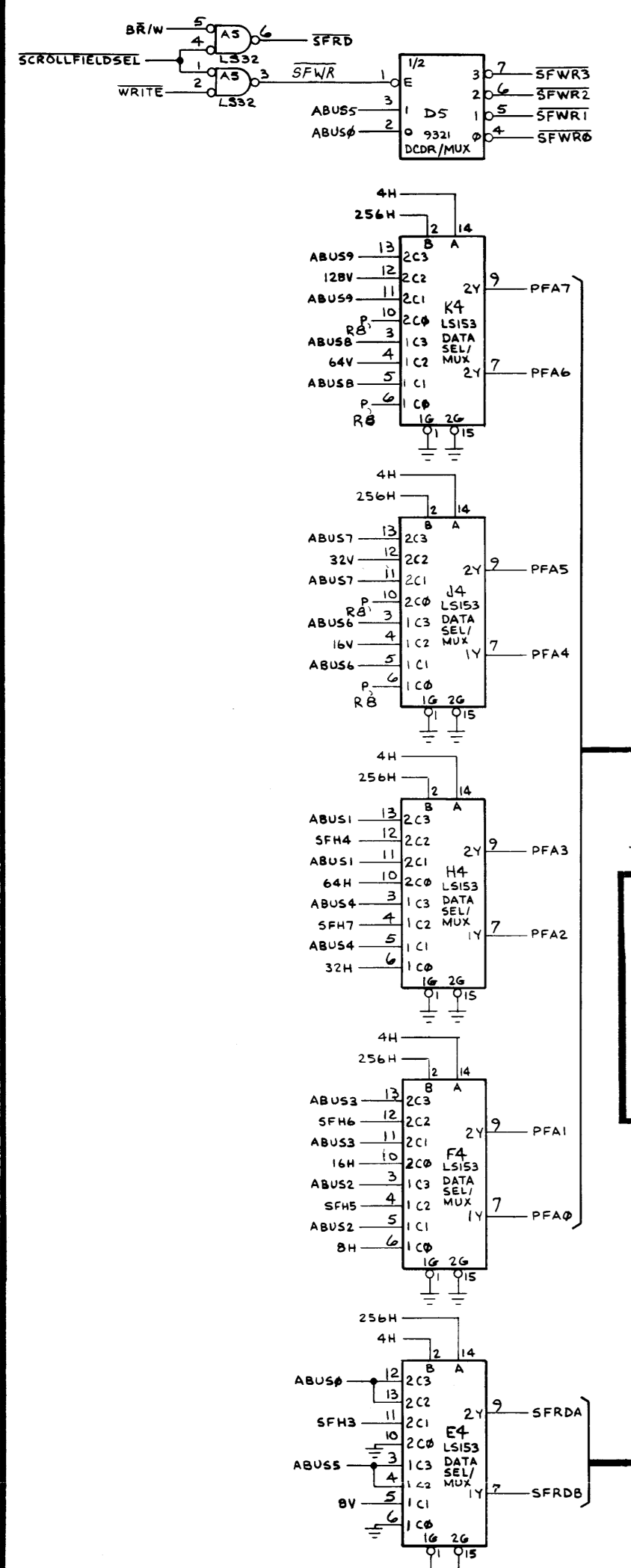


HEXADECEMAL	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0000-01FF	0	0	0	0	0	0	0	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	WORKING RAM	
0200-03FF	0	0	0	0	0	0	0	1	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	ALPHA NUMERICS	
0800-08FF	0	0	1	0	A	A	A	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	PLAYFIELD OBJECTS	
08C0-08FF	0	0	1	0	1	1	1	1	1	1	1	A	A	A	A	A	D	D	D	D	D	D	D	D	MOTION OBJECTS	
08C0-08DE	0	0	1	0	1	1	1	1	1	1	1	0	A	A	A	A	D	D	D	D	D	D	D	D	MOTION OBJECT PICTURE NUMBER	
08C1-08DF	0	0	1	0	1	1	1	1	1	1	1	0	A	A	A	A	D	D	D	D	D	D	D	D	MOTION OBJECT VERTICAL POSITION	
08E0-08FE	0	0	1	0	1	1	1	1	1	1	1	A	A	A	A	A	D	D	D	D	D	D	D	D	MOTION OBJECT HORIZONTAL POSITION	
08E1-08FF	0	0	1	0	1	1	1	1	1	1	1	A	A	A	A	A	D	D	D	D	D	D	D	D	D5, D4 AREA 3 GRAY	
08E1-08FF	0	0	1	0	1	1	1	1	1	1	1	A	A	A	A	A	D	D	D	D	D	D	D	D	D3, D2 AREA 2 GRAY	
1000	0	1	0	0	1	1	1	1	1	1	1	A	A	A	A	A	D	D	D	D	D	D	D	D	D1, D0 AREA 1 GRAY	
1001	0	1	0	0	1	1	1	1	1	1	1	A	A	A	A	A	D	D	D	D	D	D	D	D	D0 AREA 0 GRAY	
1001	0	1	0	0	1	1	1	1	1	1	1	A	A	A	A	A	0	0	0	1	W	D	D	D	CONTROL SIGNAL FOR TRACKBALL LD2	
1001	0	1	0	0	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	W	D	D	D	D	CONTROL SIGNAL FOR TRACKBALL LD1	
1001	0	1	0	0	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	W	D	D	D	D	42 PLAYER LED	
1001	0	1	0	0	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	W	D	D	D	D	SPARE	
1001	0	1	0	0	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	W	D	D	D	D	KICKER NOISE GENERATOR INITIALIZE	
1001	0	1	0	0	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	W	D	D	D	D	HIT SOUND	
1001	0	1	0	0	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	W	D	D	D	D	WHISTLE SOUND	
1002	0	1	0	0	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	W	D	D	D	D	AMP OFF	
1002	0	1	0	0	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	W	D	D	D	D	COIN COUNTER LEFT CENTER, RIGHT	
1004	0	1	0	0	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	W	D	D	D	D	INTERRUPT ACKNOWLEDGE	
1005	0	1	0	0	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	W	D	D	D	D	WATCHDOG REFRESH	
1800	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	0	R	D	D	D	D	D7 RT PLY 2 VERT DIR LD2=0, LD1=0	
1800	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	0	R	D	D	D	D	D6 RT PLY 2 HORIZ DIR LD2=0, LD1=0	
1800	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	0	R	D	D	D	D	D5 LT PLY 2 VERT DIR LD2=0, LD1=0	
1800	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	0	R	D	D	D	D	D4 LT PLY 2 HORIZ DIR LD2=0, LD1=0	
1800	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	0	R	D	D	D	D	D3 RT PLY 1 VERT DIR LD2=0, LD1=0	
1800	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	0	R	D	D	D	D	D2 RT PLY 1 HORIZ DIR LD2=0, LD1=0	
1800	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	0	R	D	D	D	D	D1 LT PLY 1 VERT DIR LD2=0, LD1=0	
1800	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	0	R	D	D	D	D	D0 LT PLY 1 HORIZ DIR LD2=0, LD1=0	
1800	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	0	R	D	D	D	D	D7-D4 RT PLY 1 VERT TRACKBALL LD2=1, LD1=0	
1800	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	0	R	D	D	D	D	D3-D0 RT PLY 1 HORIZ TRACKBALL LD2=1, LD1=0	
1800	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	0	R	D	D	D	D	D7-D4 LT PLY 2 VERT TRACKBALL LD2=1, LD1=1	
1800	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	0	R	D	D	D	D	D3-D0 LT PLY 2 HORIZ TRACKBALL LD2=1, LD1=1	
1801	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	R	D	D	D	D	ENDSCREEN	
1801	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	R	D	D	D	D	TEST	
1801	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	R	D	D	D	D	SLAM	
1801	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	R	D	D	D	D	COIN LEFT	
1801	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	R	D	D	D	D	COIN CENTER	
1801	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	R	D	D	D	D	COIN RIGHT	
1803	0	1	1	1	1	1	1	1	1	1	1	A	A	A	A	A	0	0	1	R	D	D	D	D	OPTION SWITCH	
2000-3FFF	1	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	PROGRAM SPACE	

RAM

The RAM is shared by the microprocessor and the alphanumeric generator. When Bø2 is high, the RAM is addressed by the microprocessor. When low, it is addressed by various horizontal and vertical sync signals. This process is called direct memory access, or cycle sharing.



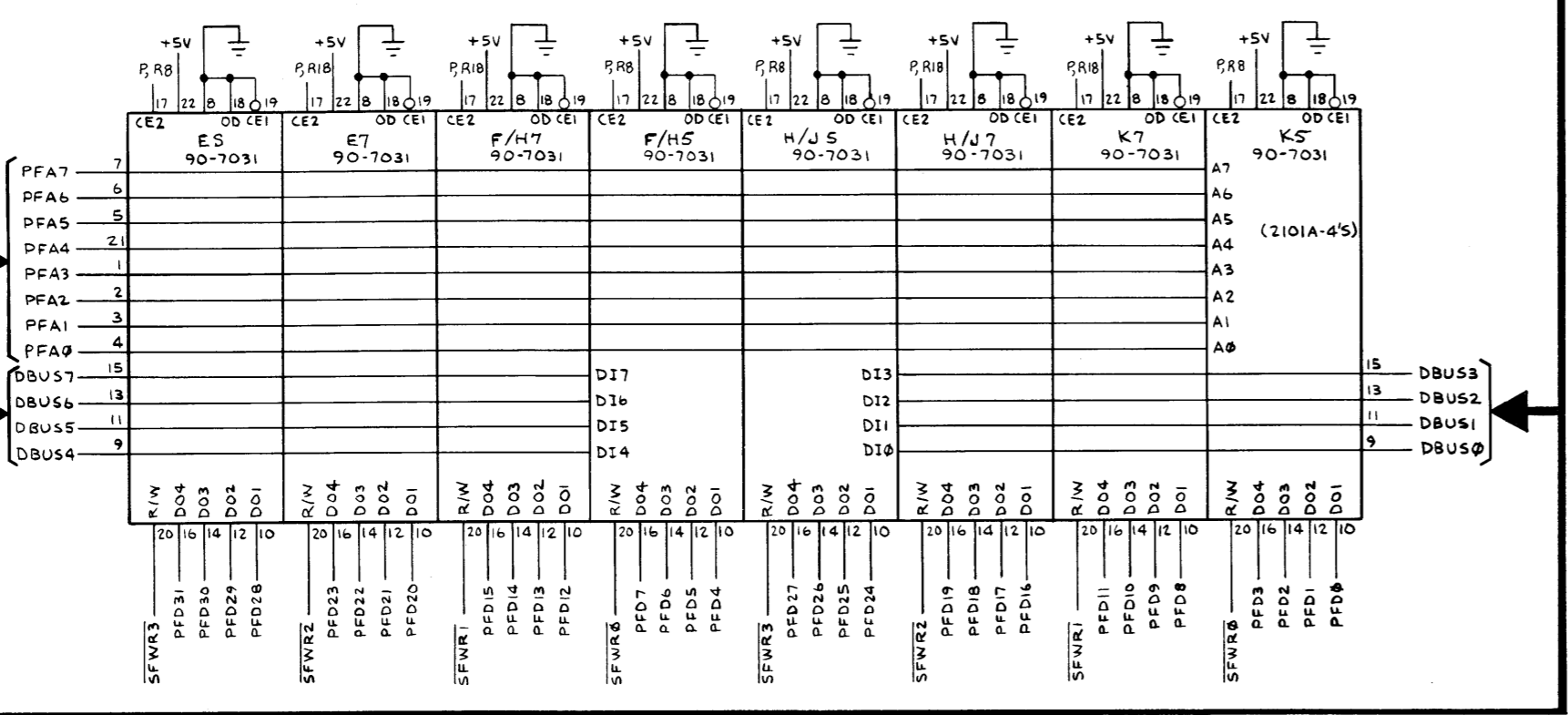


VIDEO GENERATOR

The address decoder outputs the scrollfield write enable signal SFWR, and the microprocessor selects the appropriate RAM pair with address lines ABUS0 and ABUS5.

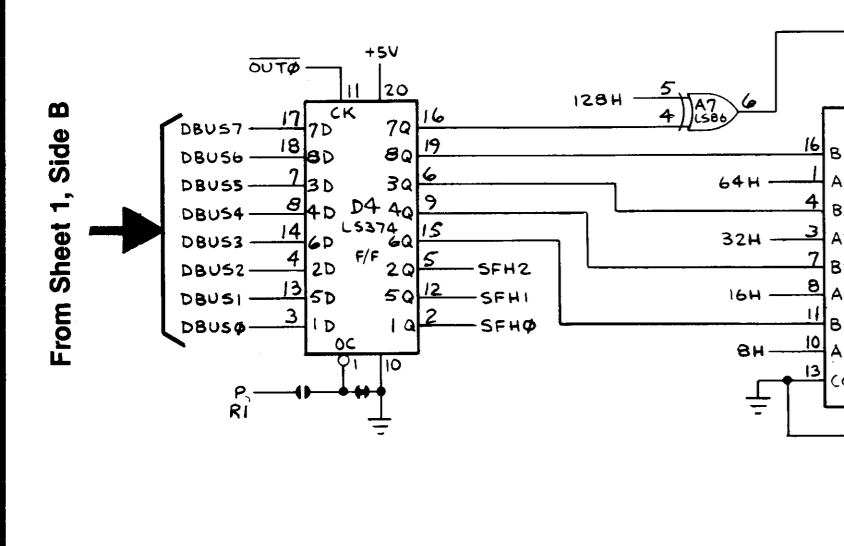
VIDEO GENERATOR RAM

When the RAM is written to by the microprocessor, SFWR is low and a RAM pair is written to by the selection of ABUS0 and ABUS5. Data is written into the RAM through data bus DBUS7. Data is read out of the RAM on data lines PFD0 thru PFD31.

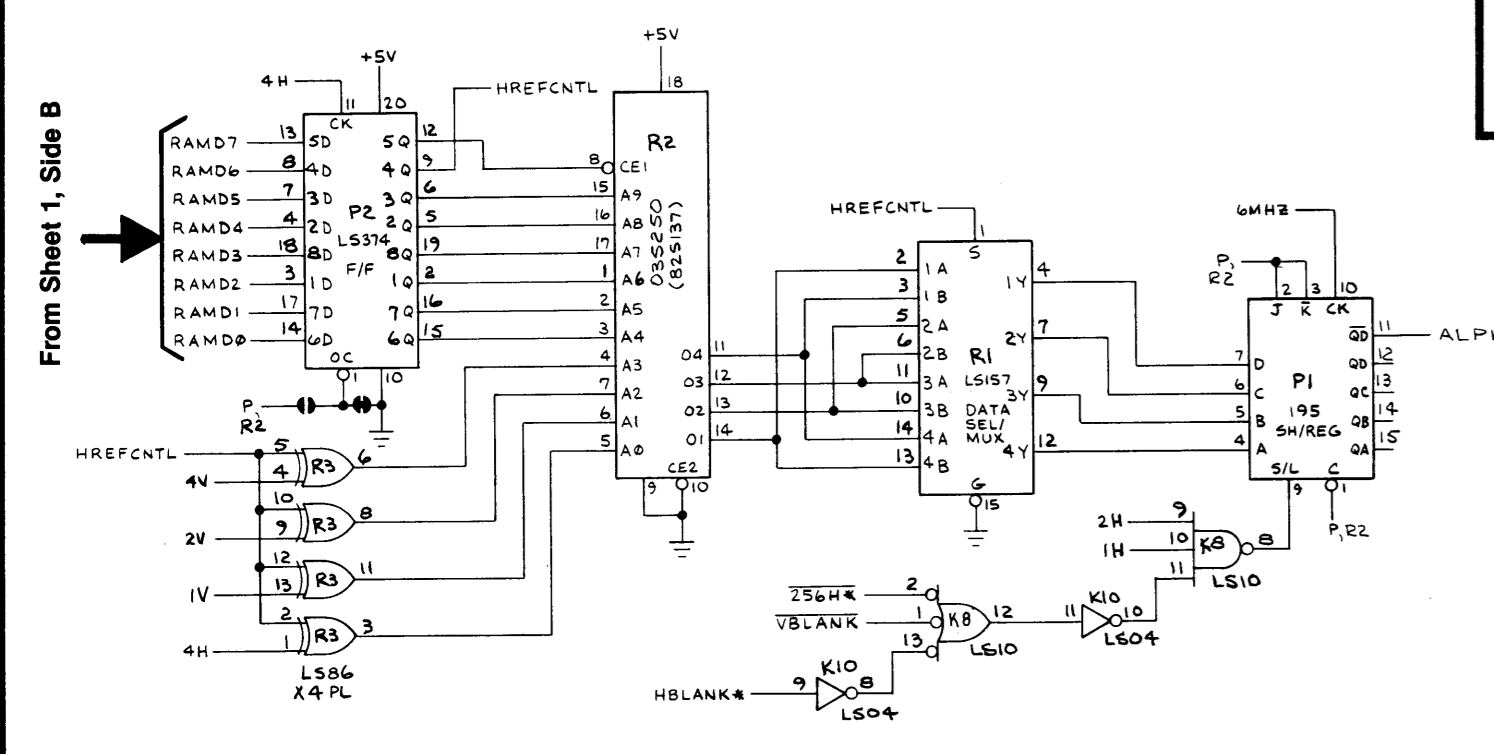


Data Selectors F4, H4, J4 and K4 select the addressing mode for the Video Generator RAM. When 4H is high, the MPU addresses the RAM, via ABUS 0-9. When 4H is low, the Video Generator RAM is addressed by either the scrollfield horizontal address (SFH 3-7) or by the sync chain (8H-64H and 16V-128V). 256H determines which of these two addresses the RAM when 4H is low. When 256H is low, sync is selected for motion objects scan. When 256H is high, scrollfield is selected.

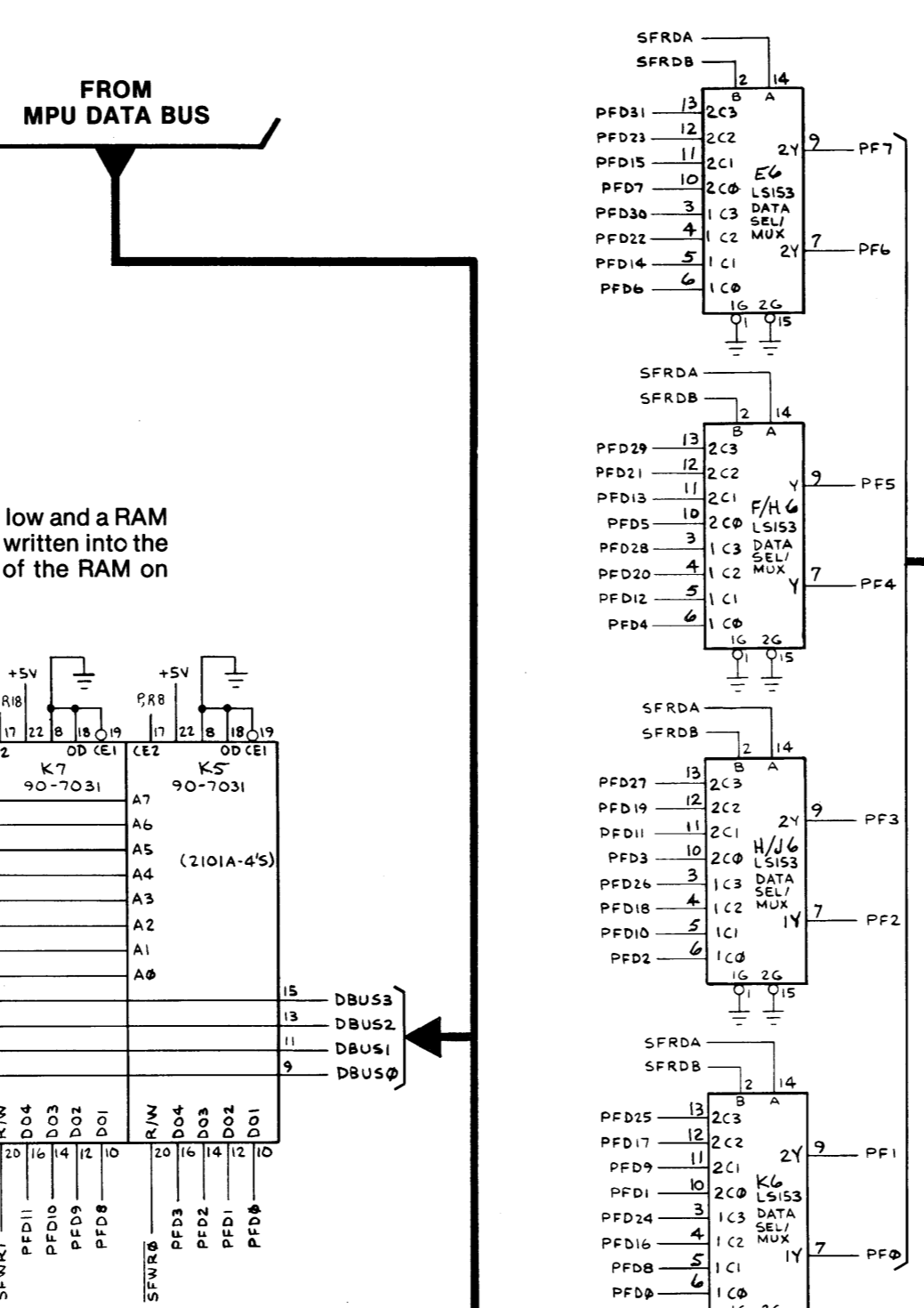
The latched data output of D4 is compared with horizontal sync 8H thru 64H, to enable the playfield to scroll (shift) in steps of 8H. SFH0 thru SFH2 selects the scrollfield output from multiplexer D6 in steps of 1H.



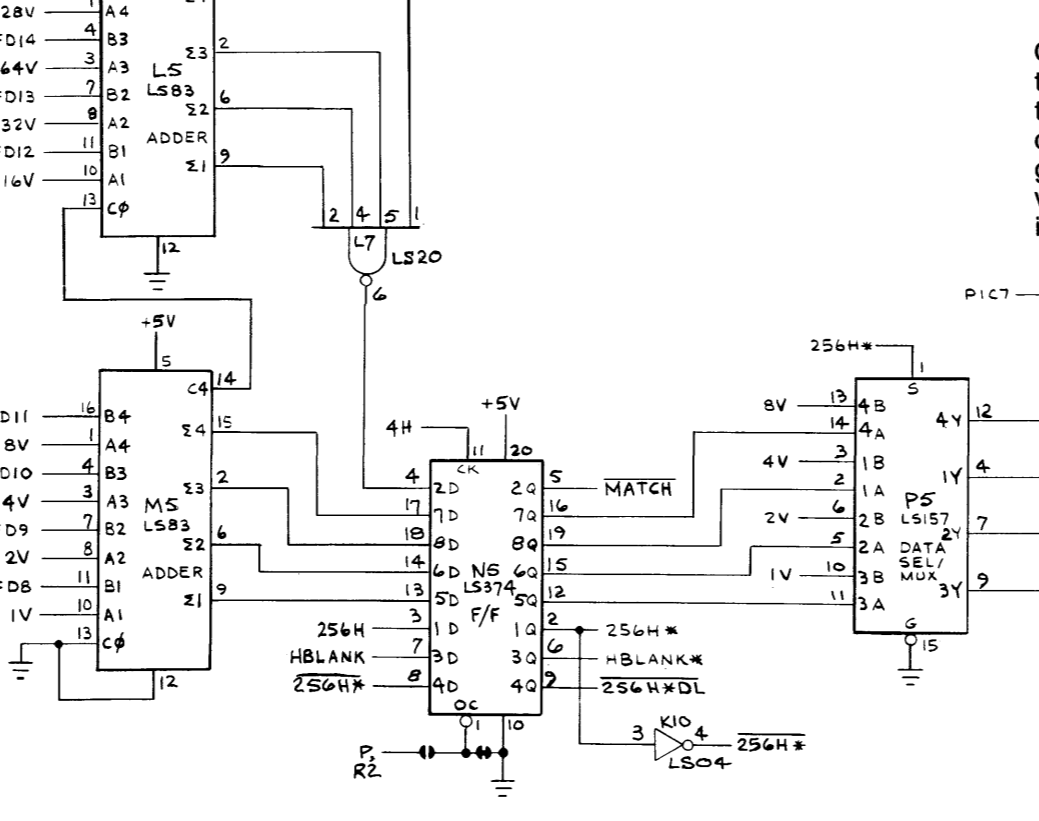
ALPHANUMERICS GENERATOR



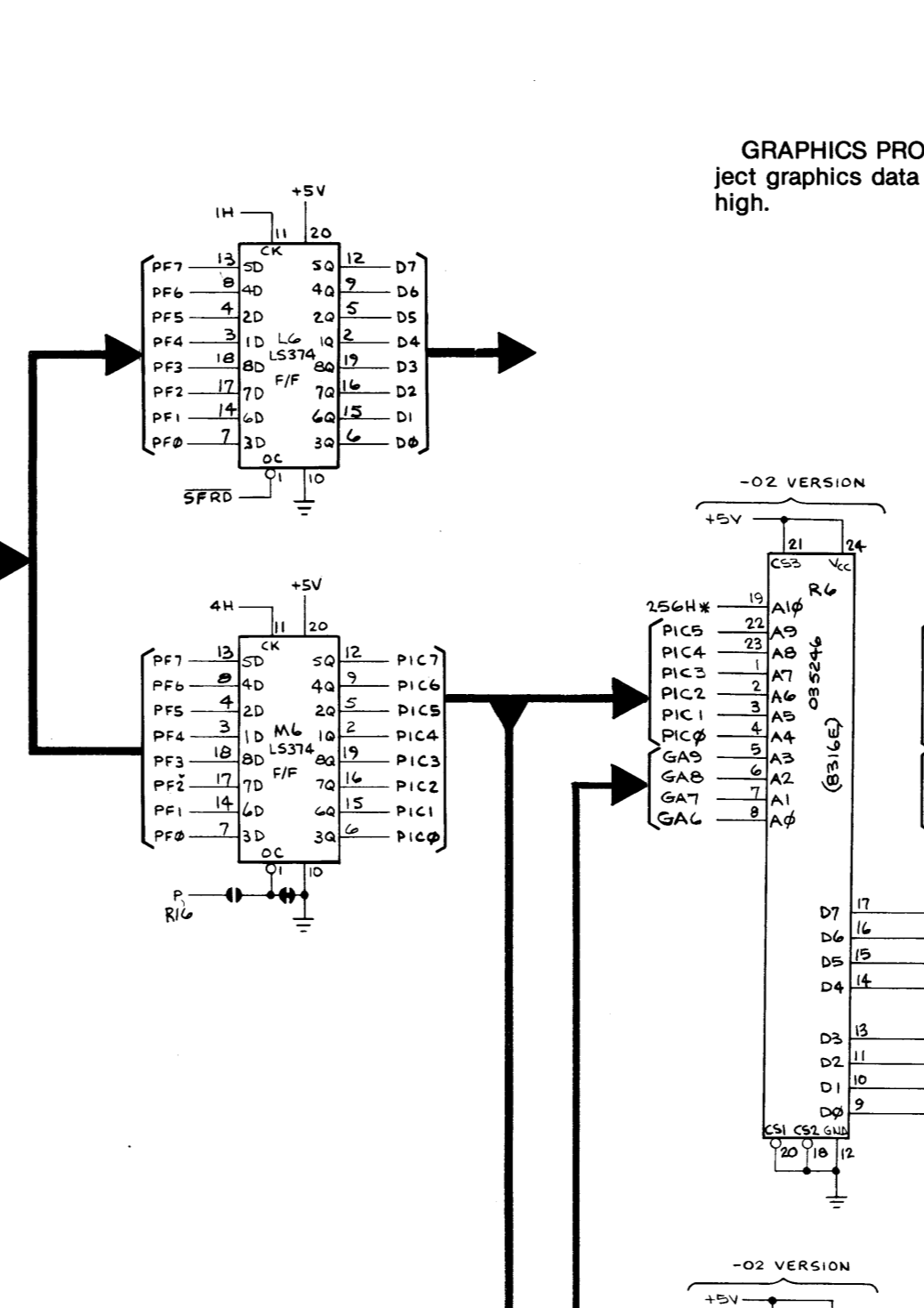
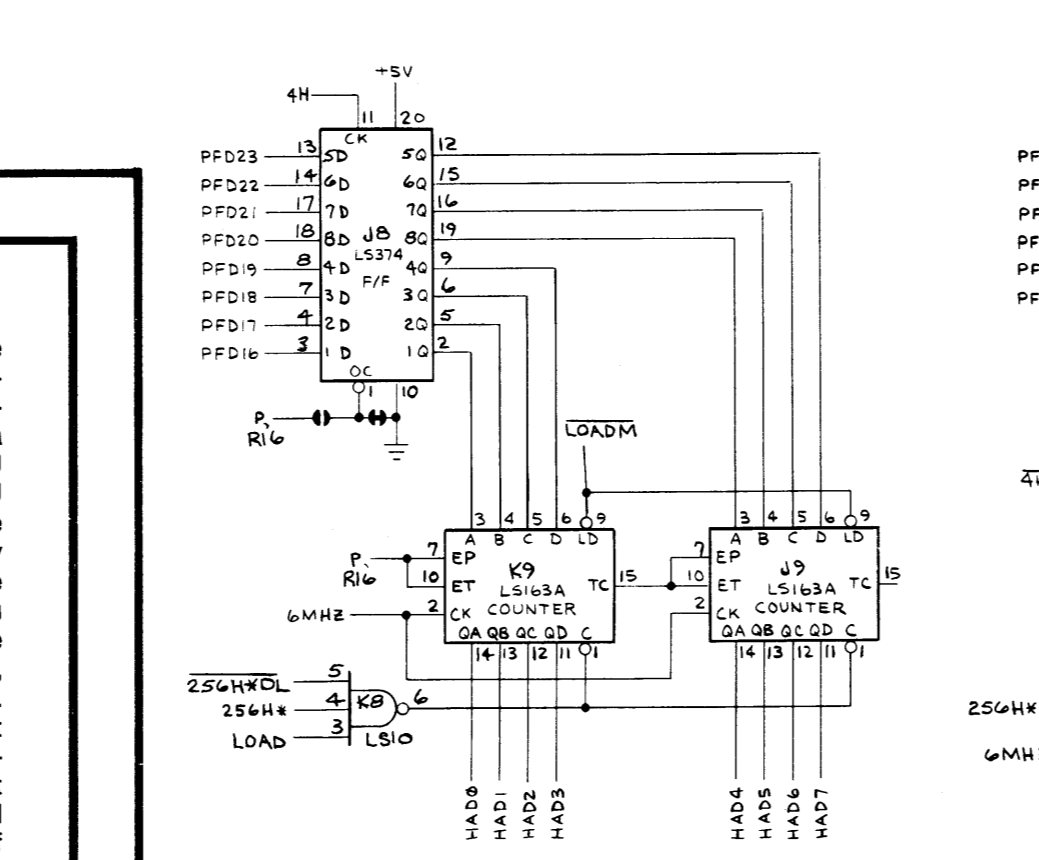
The alphanumerics at both ends of the monitor display are generated by alphanumerics PROM R2. This PROM is addressed by latched MPU RAM data signals RAMD0 thru RAMD7. The MPU writes alphanumerics data into the MPU RAM during the 92 periods. During the 92 periods the MPU RAM is accessed by horizontal and vertical sync signals. The latched MPU RAM data RAMD0 thru RAMD5, selects one of the 64 possible characters. The latched RAMD7, low data, enables the alphanumerics PROM R2. RAMD6 is used to invert the data output of the PROM both horizontally and vertically. The signal at the input of shift register P1 ensures that the generated alphanumerics only appear at each end of the monitor display.



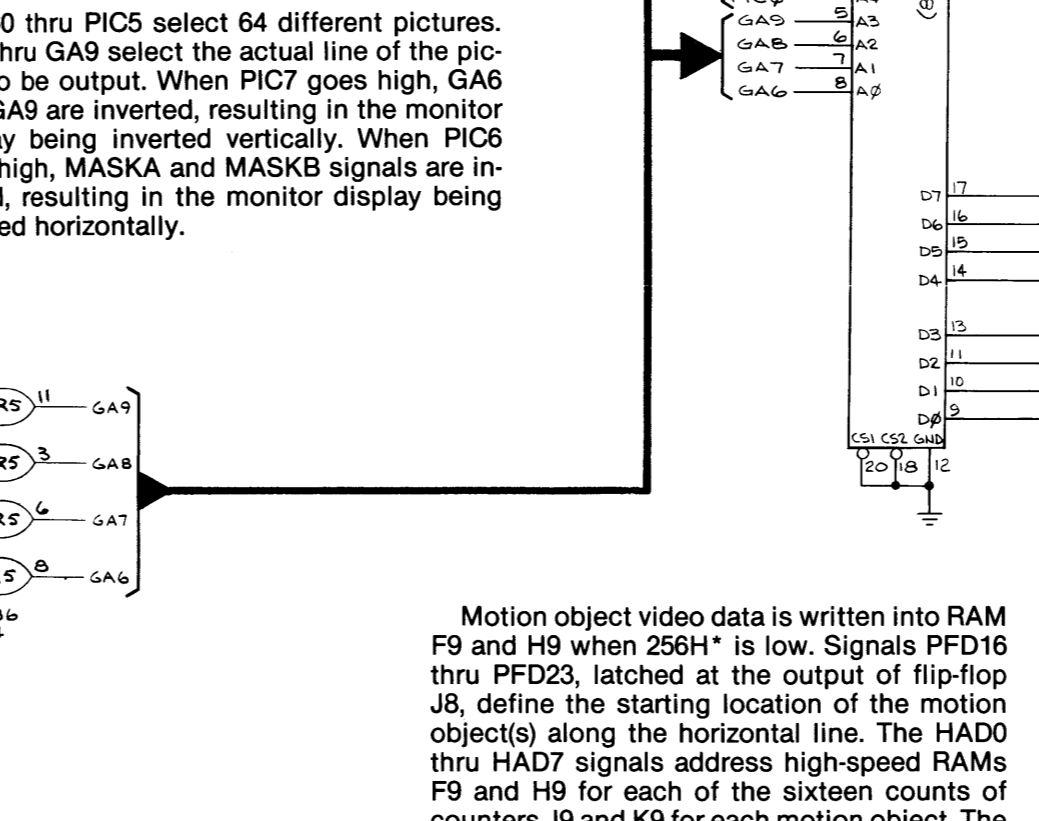
When 256* is high, playfield object graphics data is read out of Graphics ROM R6 (PROMs R7 and R8 for -01 version). During this period, the 256H* signal enables data selectors R9, P9, M8 and N8.



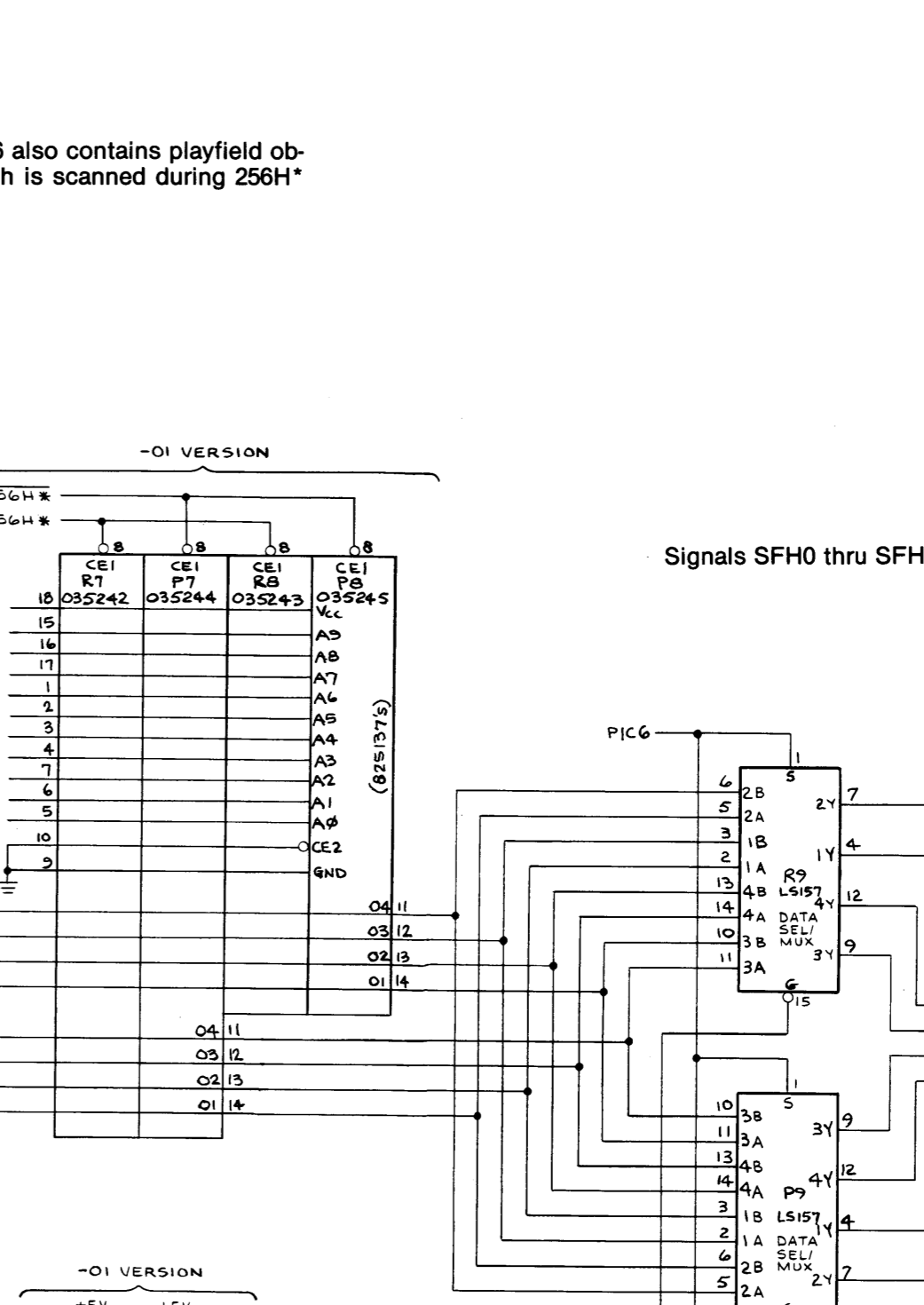
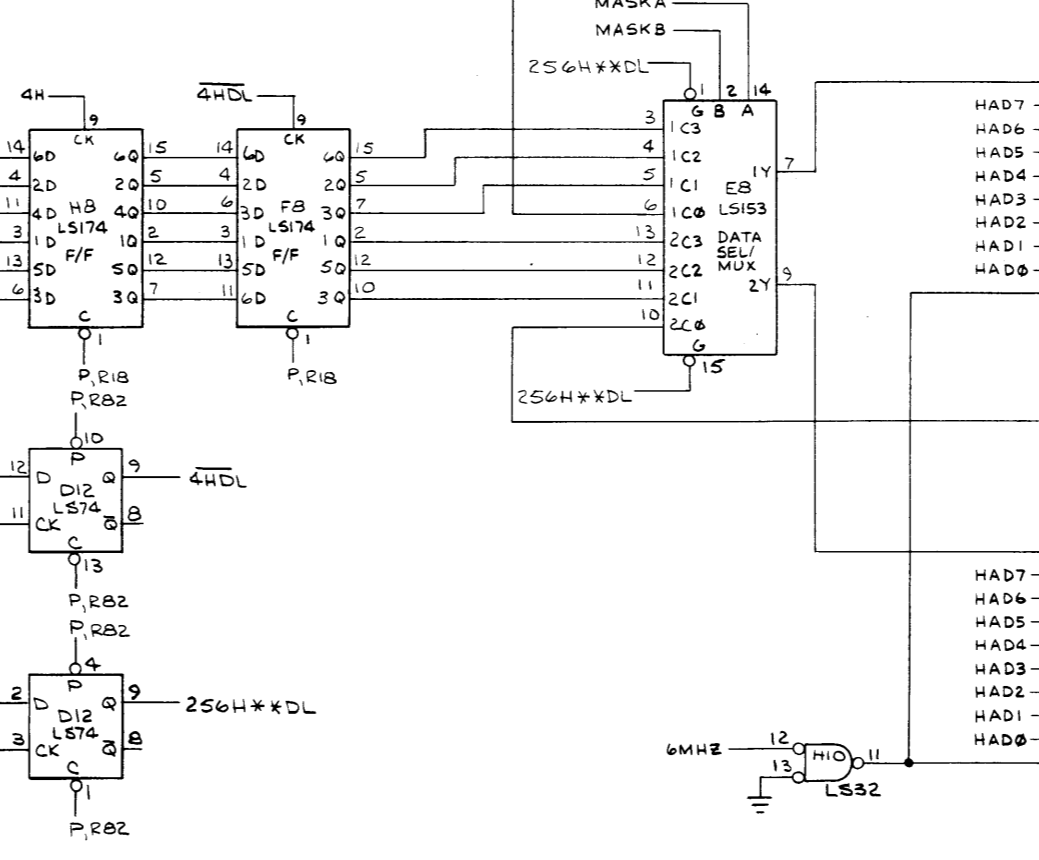
Addresses L5 and M5 compare the vertical line presently being scanned with RAM data PFD8 thru PFD15, which defines the vertical location of the motion object. When the inputs are equal, MATCH is latched low, permitting the motion object data to be output from the graphics PROM. GA6 thru GA9 count up for the 16 scan lines of the motion object picture during 256H* low, otherwise it passes vertical count 1V thru 8V during 256H* high for playfield scan.



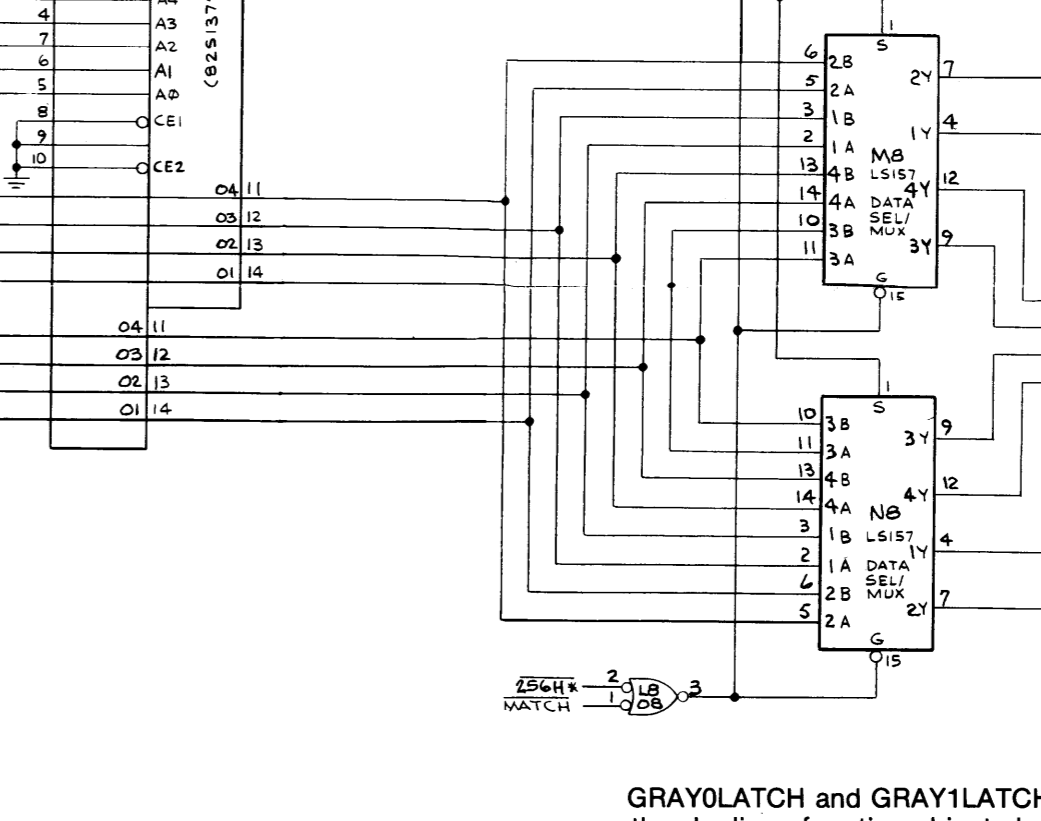
PIC0 thru PIC5 select 64 different pictures. GA6 thru GA9 select the actual line of the picture to be output. When PIC7 goes high, GA6 thru GA9 are inverted, resulting in the monitor display being inverted vertically. When PIC6 goes high, MASKA and MASKB signals are inverted, resulting in the monitor display being inverted horizontally.



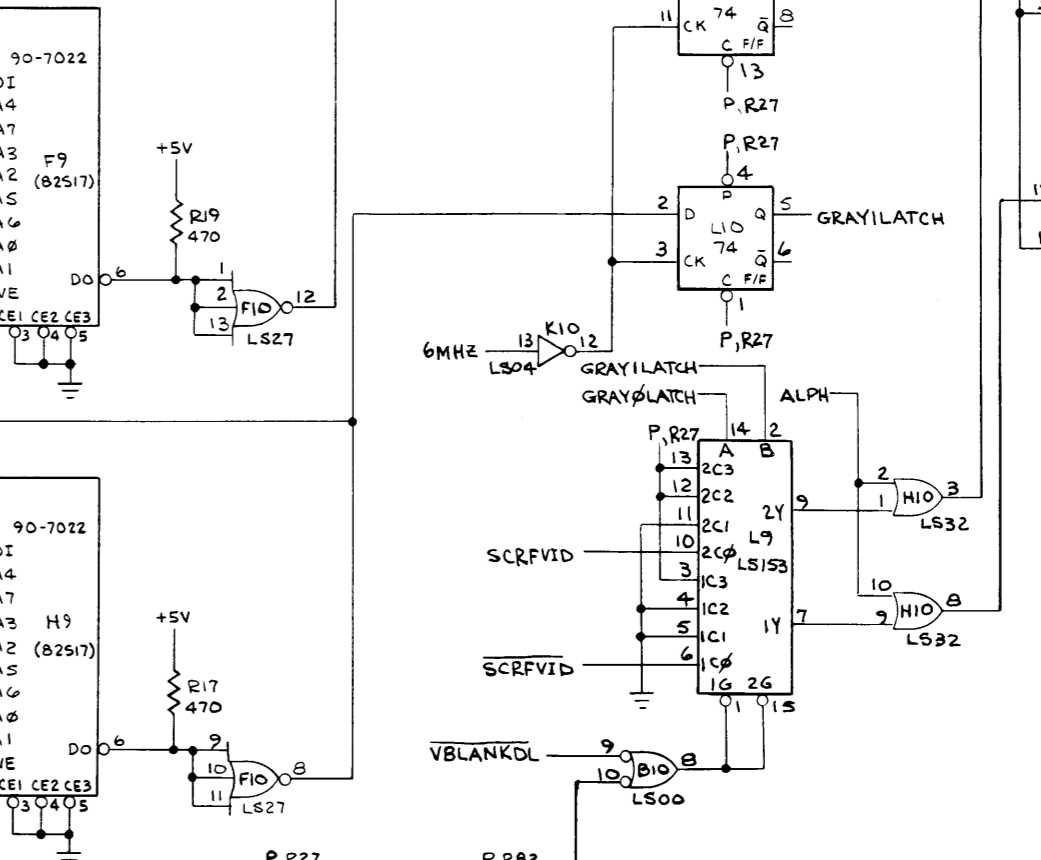
Motion object video data is written into RAM F9 and H9 when 256H* is low. Signals PFD16 thru PFD23, latched at the output of flip-flop J8, define the starting location of the motion object(s) along the horizontal line. The HAD0 thru HAD7 signals address high-speed RAMs F9 and H9 for each of the sixteen counts of counters J9 and K9 for each motion object. The data written into the RAMs is color coded by the selection of signals PFD24 thru PFD29 selected by MASKA and MASKB through multiplexer E8.



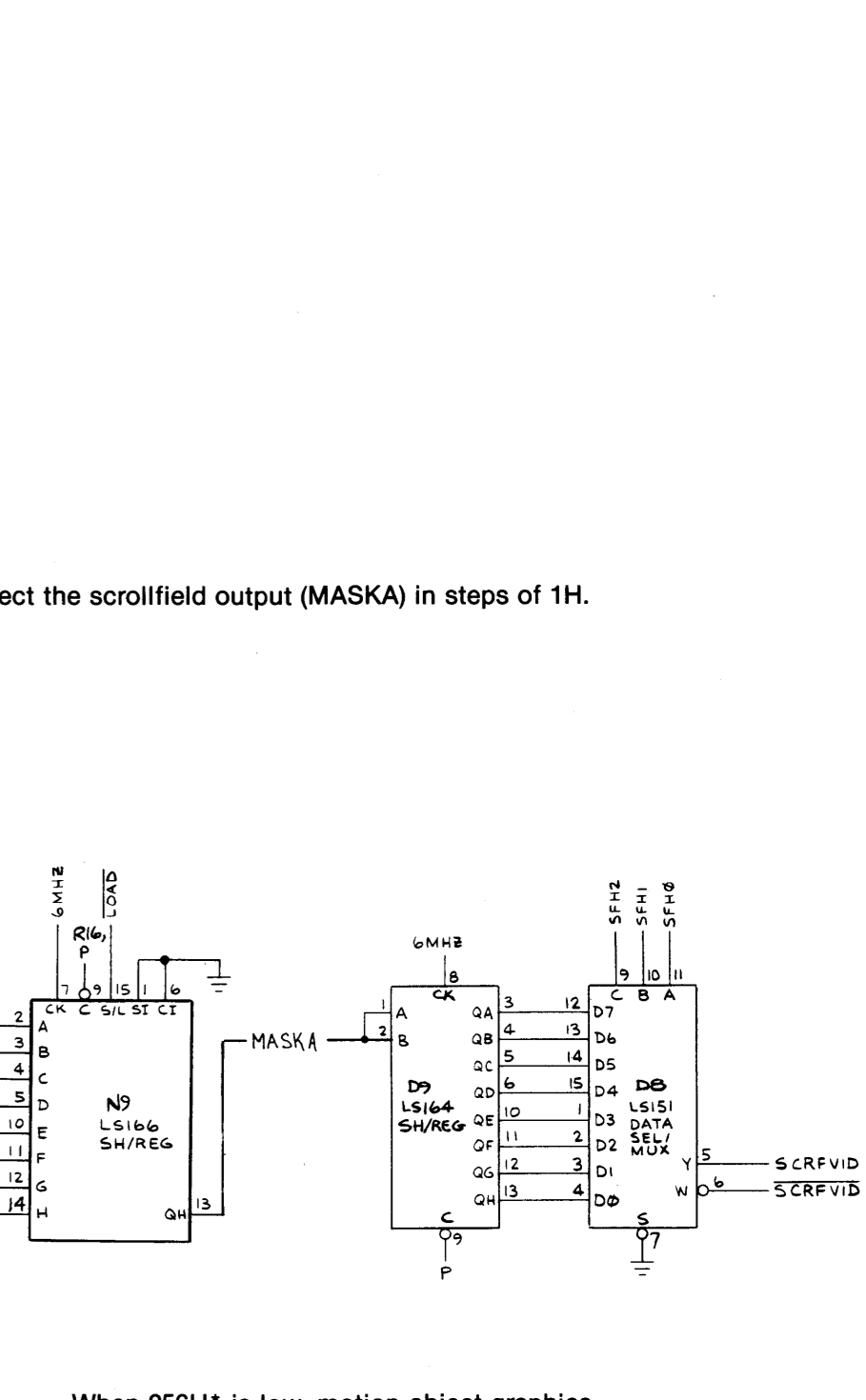
At the beginning of the actual scan line, the counters are cleared and start counting from 0 to 255. Data written into RAMs F9 and H9 are read out of locations addressed by HAD0 thru HAD7.



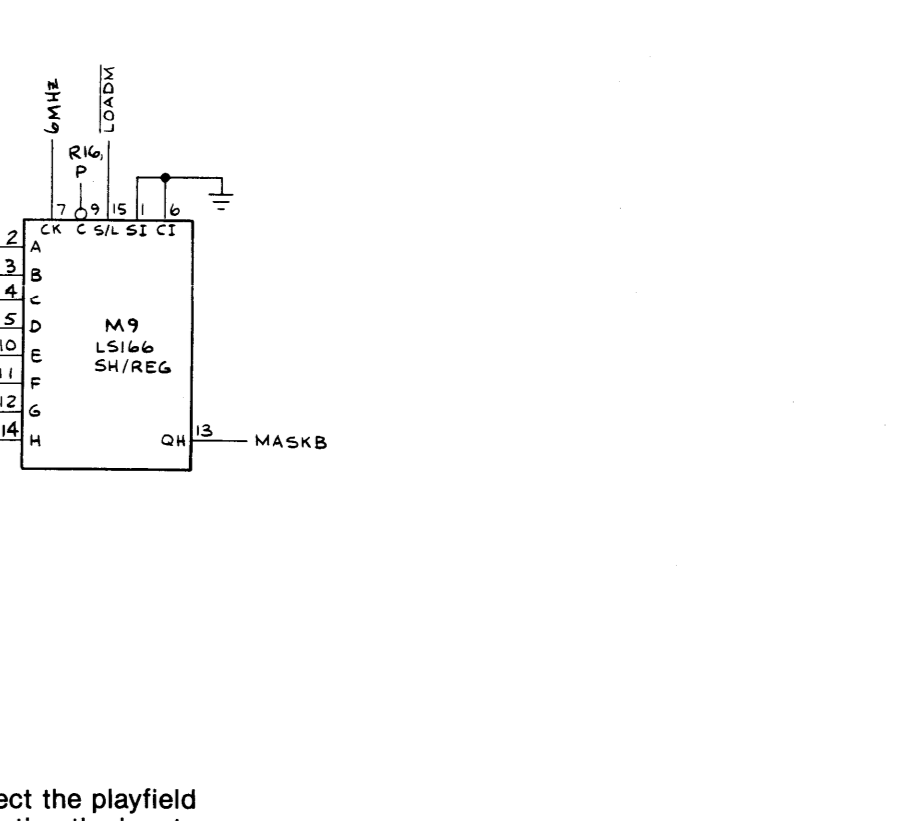
GRAY0LATCH and GRAY1LATCH select the playfield or the shading of motion objects by selecting the inputs of multiplexer L9. When both GRAY0LATCH and GRAY1LATCH are low, playfield objects are output. When GRAY0LATCH is high and GRAY1LATCH is low, black motion objects are output. When GRAY0LATCH is low and GRAY1LATCH is high, gray motion objects are output. When GRAY0LATCH and GRAY1LATCH are both high, white motion objects are output.



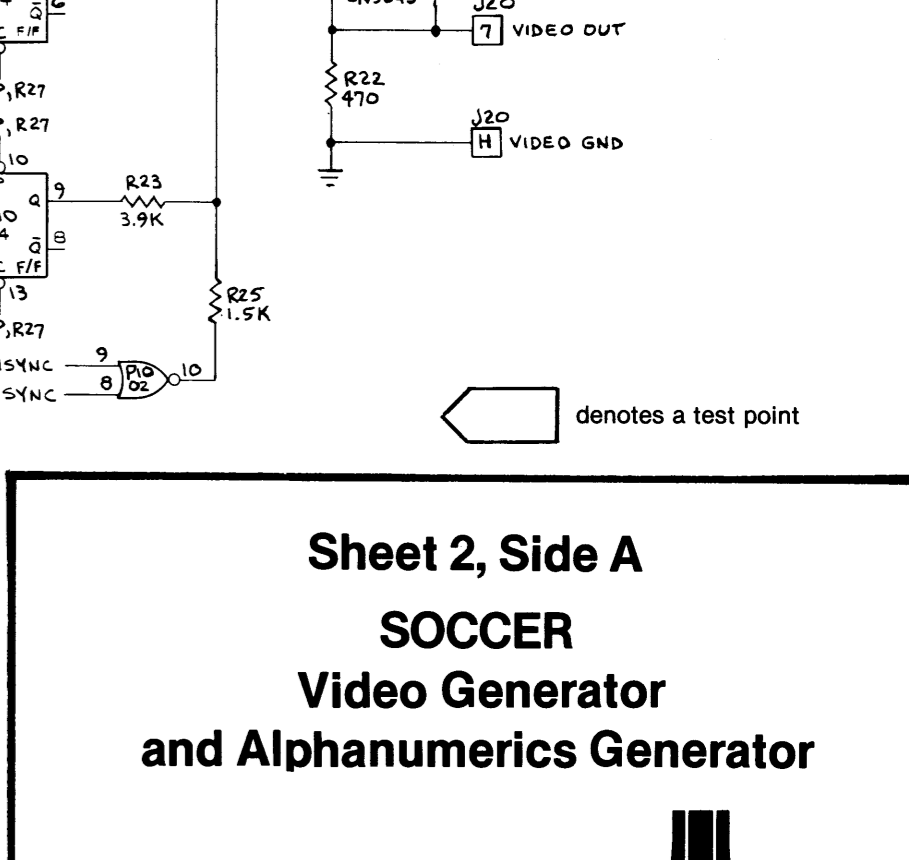
The alphanumerics, playfield, motion objects video and vertical and horizontal sync signals are all summed at the video summer. The VBLANKL signal ensures that there is no video during the vertical blanking period.



When 256H* is low, motion object graphics data is read out of Graphics ROMs, R6 and N6 (PROMs R7, R8, P7, P8, N7 and M7 for -01 version) when MATCH is low. MASKA and MASKB define different areas of the motion object picture. The actual shading of the picture is assigned later with PFD25 thru PFD28 by multiplexers E8 and L9.

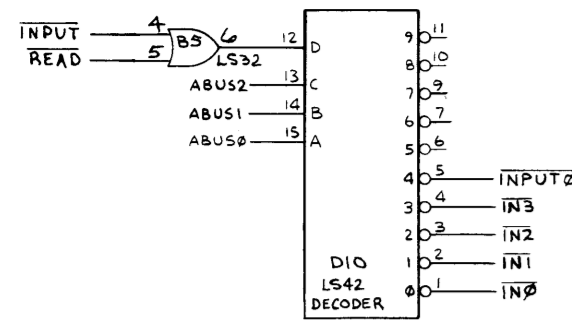


Signals SFH0 thru SFH2 select the scrollfield output (MASKA) in steps of 1H.



denotes a test point

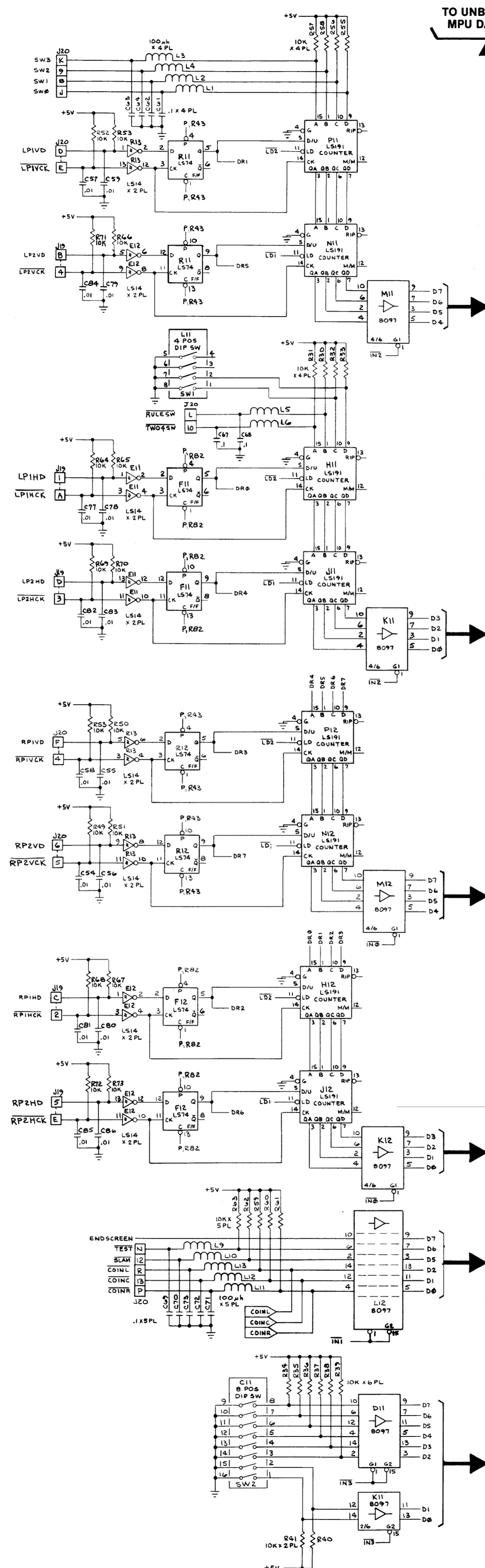
SWITCH and TRAK BALL INPUTS



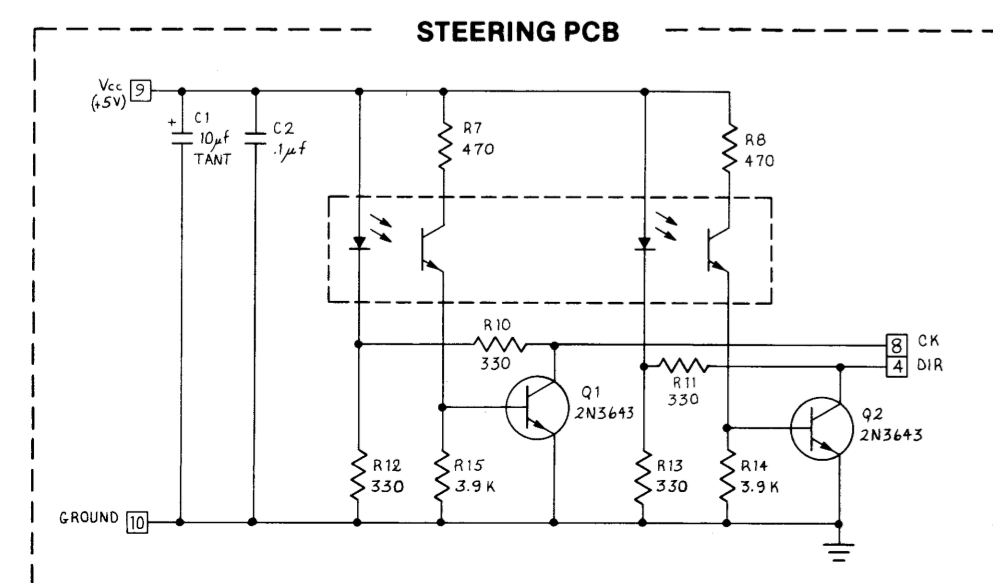
- The sequence for reading the RULESW, TWO4SW, and 4-position DIP option switch and kick buttons are as follows:
- LD1 and LD2 are latched low at the output of D6 on the rising edge of OUT1.
 - IN2 from the address decoder enables input ports K11 and M11.
 - The microprocessor reads the switches on data lines D0 to D7 through counters J11, H11, N11 and P11.

The Trak Balls are read by the microprocessor through input ports K11, M11, K12 and M12. Ports K11 and M11 are enabled by IN2 from the address decoder, and K12 and M12 are enabled by IN0. When LD1 and LD2 are both high, the microprocessor reads the rate of turn for the Trak Balls connected to J12 and N12, or connected to J11 and N11. When LD1 is low and LD2 is high, the microprocessor reads the rate of turn for the Trak Balls connected to the input of counters H12 and P12, or H11 and P11. When LD1 and LD2 are both low, the microprocessor reads the direction of the "PLAYER 2" Trak Balls on data lines D4-D7, and the "PLAYER 1" Trak Balls on data lines D0-D3.

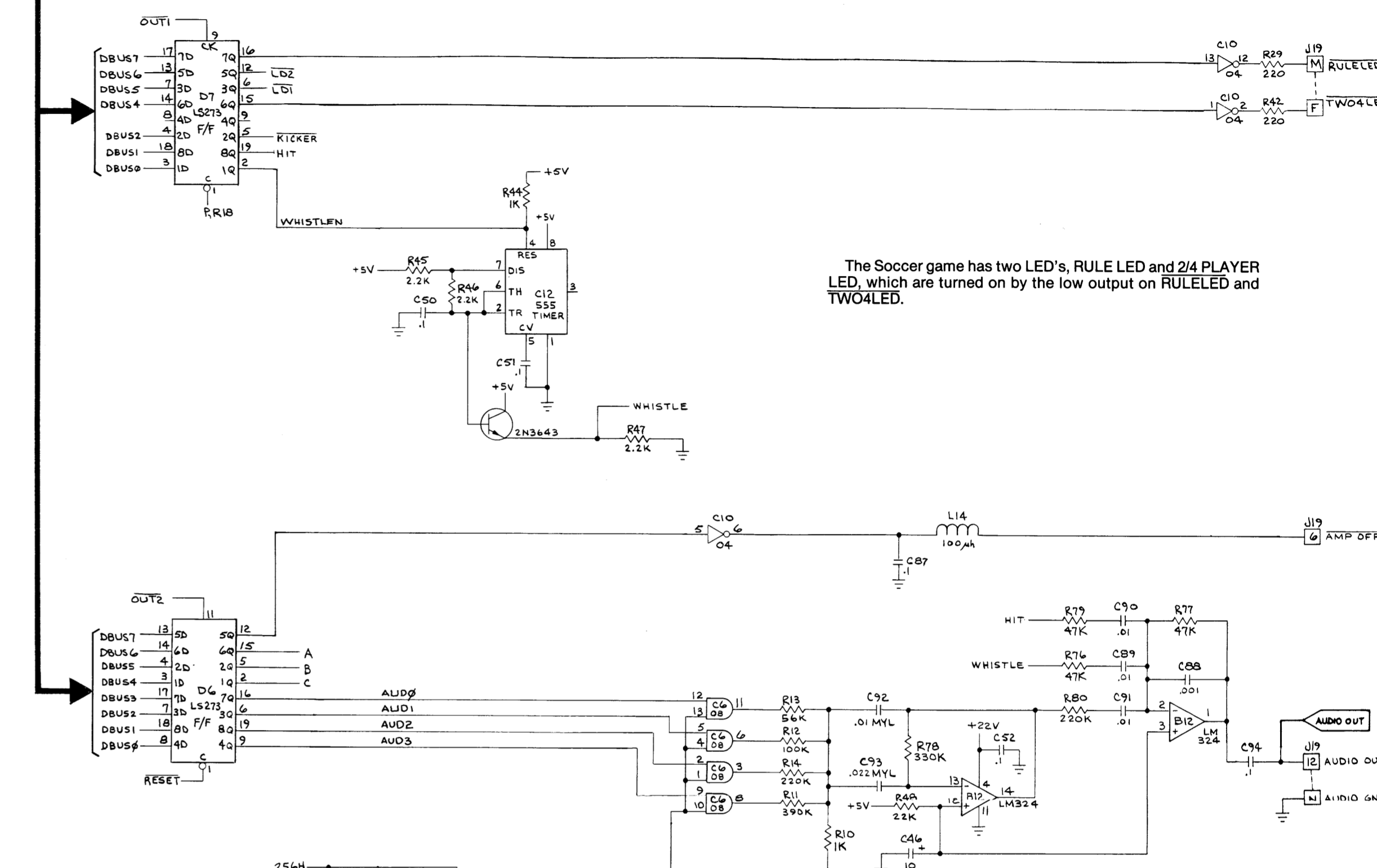
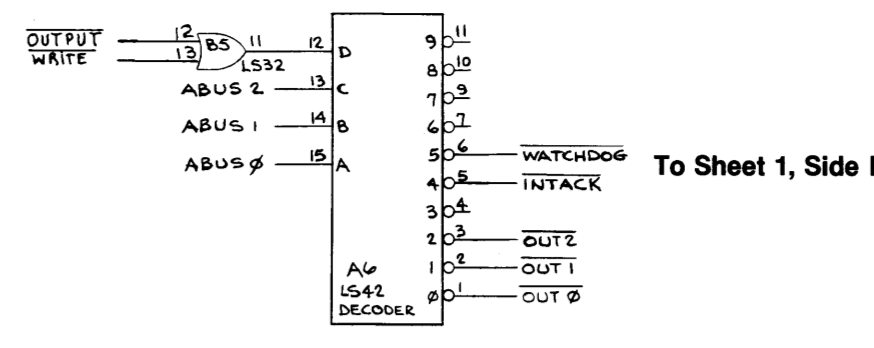
The option switch toggles are read on data lines D0 thru D7 when IN3 from address decoder enables input ports D11 and K11.



Coin slam and self-test switch inputs are connected to +5 VDC through pullup resistors. When a switch is closed, that input is pulled to ground. The switch is read by the microprocessor when switch input port L12 is enabled by IN1 from the address decoder.



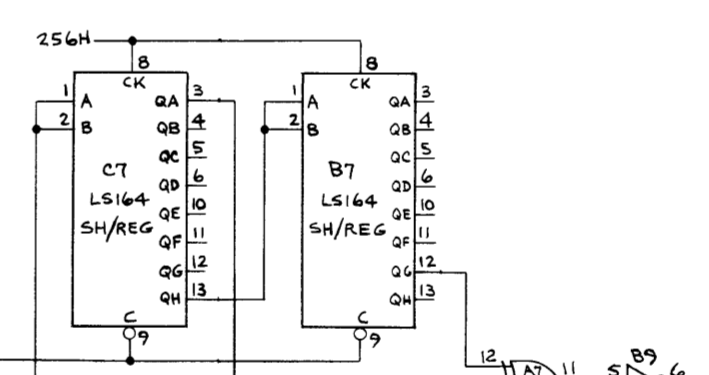
AUDIO, LED, and COIN COUNTER OUTPUTS



The Soccer game has two LED's, RULE LED and 2/4 PLAYER LED, which are turned on by the low output on RULELED and TWO4LED.

The audio generator generates the crowd, hit, and whistle sounds. The crowd sound is generated from random noise from B7 and C7. The volume of the crowd sound is controlled by the AUD0 thru AUD3 data latched at the output of D6. Hit is enabled by the HIT data latched at the output of D7. (A "hit" occurs when the ball is kicked).

Whistle is enabled by WHISTLEN data from the output of latch D7. The amplifier is enabled when AMPOFF from latch D6 is high.



Coin counters are activated by low outputs on COIN CNTRL, COIN CNTRC and COIN CNTRR which are controlled by the latched outputs A, B and C, from D6.

Option Switch Settings

To change toggle positions of the switch assemblies, you need not remove the game PCB. The switches, usually colored blue, are easily accessible when the PCB is mounted in place. When changing the options, verify proper results on the TV monitor display during self-test.

Toggle settings of 8-toggle switch on game PCB				Option	TV Monitor Display During Self-Test					
8	7	6	5	4	3	2	1			
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	OFF OFF OFF	4:00 per credit	Three digits of first line immediately below ROM OK message (picture below indicates time setting of 1:00 per credit)
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	OFF OFF ON	3:30 per credit		
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	OFF ON OFF	3:00 per credit		
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	OFF ON ON	2:30 per credit		
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	ON OFF OFF	2:00 per credit		
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	ON OFF ON	1:40 per credit		
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	ON ON OFF	1:20 per credit	Left coin mech multiplied by 1 Left coin mech multiplied by 2	
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	ON ON ON	1:00 per credit		
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	ON ON	Right coin mech multiplied by 1 Right coin mech multiplied by 4 Right coin mech multiplied by 5 Right coin mech multiplied by 6	Third digit of second line below ROM OK message (picture below indicates 5 time credits per coin).	
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	ON OFF	Right coin mech multiplied by 1 Right coin mech multiplied by 4 Right coin mech multiplied by 5 Right coin mech multiplied by 6		
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	OFF ON	1 coin minimum	Single digit in third line below ROM OK message (picture below indicates 1 coin minimum).	
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	OFF OFF	2 coin minimum		

Toggle setting of 4-position switch on game PCB				Language
4	3	2	1	
N	O	O	N	English
O	O	N	O	German
O	T	O	O	French
U	S	E	F	Spanish



Sheet 2, Side B
SOCCER
Switch Inputs, Audio, Coin Counter, and LED Outputs
034905-XX A

